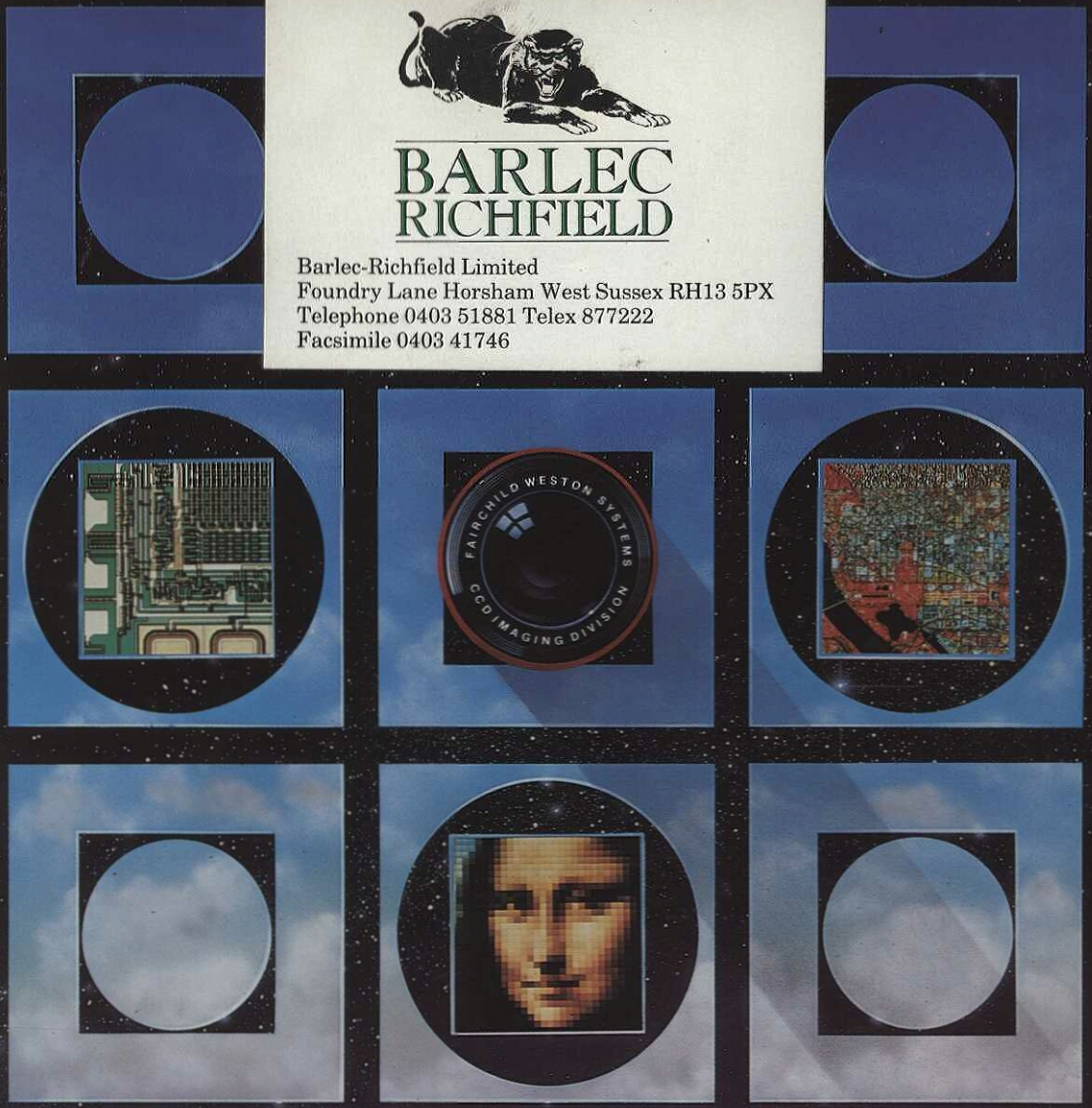


BARLEC
RICHFIELD

Barlec-Richfield Limited
Foundry Lane Horsham West Sussex RH13 5PX
Telephone 0403 51881 Telex 877222
Facsimile 0403 41746

1987
CCD Solid State Imaging Technology

FAIRCHILD WESTON
Schlumberger

1987
CCD Databook

CCD Solid State Imaging Technology

FAIRCHILD WESTON

CCD IMAGING DIVISION

CCD Imaging and Signal Processing Catalog and Applications Handbook

Fairchild Weston Systems, Inc. CCD Imaging Division.
810 W. Maude Ave., Sunnyvale, California 94086
(408) 720-7600, TWX 910-373-2110

Manufactured under one of the following U.S. Patents: 2981877, 3015048, 3064167, 3108359, 3117260; other patents pending.

Table of Contents

L'Enfant's street plan for Washington, D.C. **(above)** *approximating Paris, is obvious in this view made by the French SPOT Image Corporation's remote sensing satellite system . . a system which relies on CCD technology. Fairchild Weston's CCD Imaging Division was a supplier to SPOT.*

Created for commercial and environmental applications, SPOT is able to "see" 1400 square miles in one 10-second pass, or more than 25 conventional high-altitude aerial photographs.

Aerial photography, itself, was made possible by the inventions of Sherman Mills Fairchild—shutter and timing mechanisms, camera systems and closed-cabin aircraft **(right).**

Fairchild founded several companies which evolved leadership roles in aircraft development, defense electronics & systems, optics, semiconductor manufacturing, as well as CCD Imaging Technology.

The Fairchild Evolution of CCD Imaging

The Fairchild CCD Imaging Division, which successfully developed and delivered the first commercial charged-coupled device in 1973, actually traces its roots back through two branches of the corporate tree to the noted American inventor, scientist and industrialist, Sherman Mills Fairchild in the early 1920's.

Fairchild's first invention was an efficient between-the-lens camera shutter and associated timing mechanism which enabled accurate aerial photography for the first time.

Fairchild's additional inventions in aircraft technology (including the first enclosed cabin airplane, the first with folding wings, the first with hydraulically-operated landing gear and brakes) were consolidated into the Fairchild Aviation Corporation.

In 1936, aircraft products were separated from the camera related operations in New York as the Fairchild Engine and Airplane Corporation in Maryland.

Fairchild Camera & Instrument Corporation
During World War II, the New York photography operation designed and manufactured 90 percent of the aerial cameras used by all Allied forces, and the firm adopted the name Fairchild Camera and Instrument Corporation.

After the war, products related to the original camera manufacturing operations made Fairchild a major US government supplier of aerial cameras, surface surveillance systems and other defense related products.

Fairchild Semiconductor
In the late 1950's, the company sponsored a small group of young scientists in California developing new processes for the manufacture of transistors.

Their goal was to develop, mass produce and market semiconductor components that could meet the most stringent customer requirements, and in 1959 the Planar process was introduced.

By the mid-70's Fairchild had become the third largest US supplier of semiconductors, and the parent, Fairchild Camera & Instrument Corp., was all but eclipsed by the offspring Semiconductor Division and its accelerating technology.

For example, at the Palo Alto Research Lab, a major effort was being made to advance CCD imaging technology and to speed process development of manufacturing a broad range of solid-state sensing devices.

Meanwhile in Syosset, New York, the company was introducing a panoramic aerial camera with an exclusive rotating optical prism, making possible the first 180-degree, horizon-to-horizon aerial photograph.

Schlumberger Limited
In 1979, Fairchild became a part of Schlumberger Limited, a company which, like Fairchild, had grown successfully through innovations in science and industry.

Shortly after the turn of the century, brothers Conrad and Marcel Schlumberger's experiments with surface electrical instruments led to an "electric log" process for French oil exploration that demonstrated conclusively that geological formations penetrated by the drill could be identified by electrical measurements.

Today, Schlumberger is an international company providing oil and gas drilling and production services; energy measurement and control equipment; instruments, components and computer-aided design; and manufacturing and control systems.

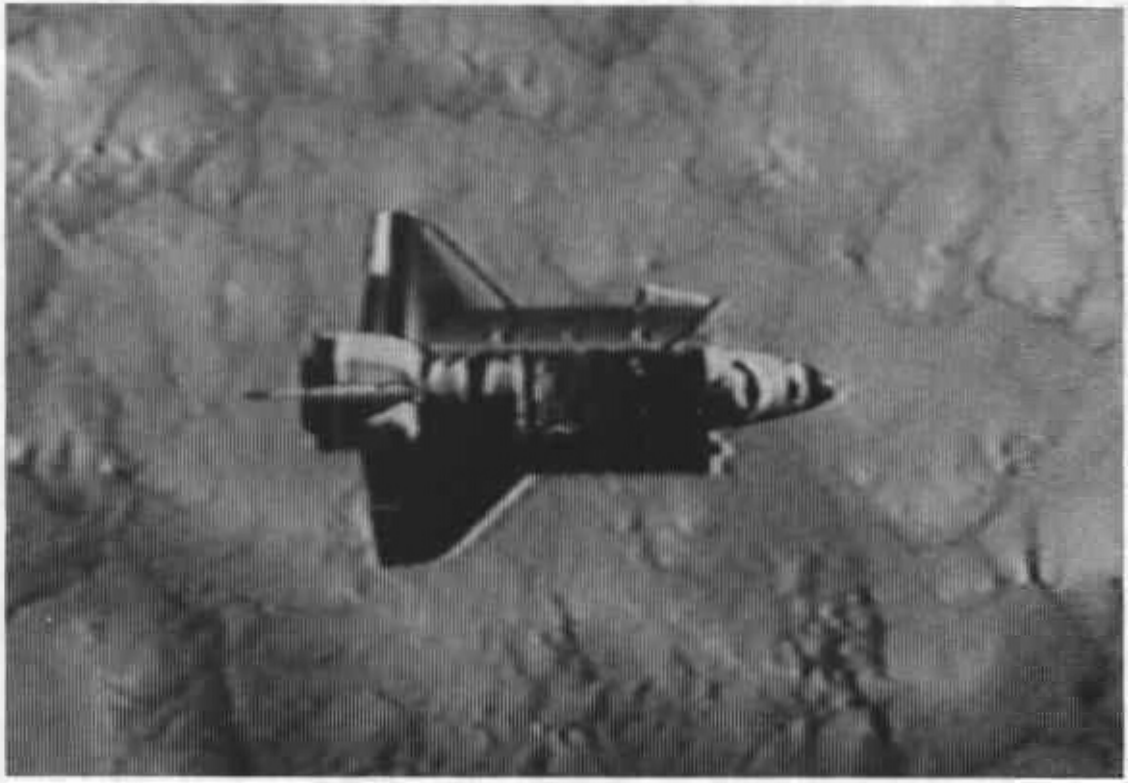
Fairchild Weston Systems, Inc.
Fairchild Weston Systems, descendant of the former Fairchild Camera & Instrument Corporation, continues to carry the mantle of the original camera operation and to expand its technology base as world leader in the design, development and fabrication of high technology electronic, photographic and electro-optical systems for defense-related applications.

CCD Imaging Division
The original buried-channel CCD product technology was transferred from the R&D operation to the CCD Imaging volume production environment late in the 1970's with the requisite efforts in development and production engineering in order to produce a full line of linear and area sensors, cameras and camera subsystems as well as ancillary devices in signal processing and interface systems.

In 1985, CCD Imaging was incorporated into the Electro-Optical Systems Group of Fairchild Weston as a natural complement to the continuing program of solid-state TV camera development for NASA and other high-technology users. The first pictures ever taken of a space shuttle in orbit were made by a Fairchild Weston miniature color TV camera mounted on a pallet satellite.

Today, Fairchild Weston's CCD Imaging Division provides sophisticated devices and systems for inspection, measurement, surveillance, telecine, facsimile and optical character recognition in industry, science, medicine, defense and many other fields.

In numerous applications—from food processing to astronomy, from robotics to cartography—the CCD Imaging Division continues to spearhead the CCD technological revolution with a wide selection of devices and camera systems.



Custom Engineering Services
The CCD Division's technical staff of highly experienced engineers is available for special requirements in several areas.

CCD Custom Specifications
The performance levels of standard products have been chosen to meet most applications. However, some systems may require devices with tighter specifications —lower dark signals, more uniform photoresponse, higher responsivity or some other parameter not included in a standard product.

Custom & Semicustom Options
Infrared Performance
Silicon CCD photosites are optimized for visible light (400-700nm). Although silicon photosites have substantial responsivity in the near-IR (700-400nm), spatial resolution (MTF) degrades severely as wavelength decreases beyond about 700nm. Maximum useable wavelengths are generally in the 800-900nm range. Many light sources (tungsten lamps, sunlight, etc.) have strong IR components. Hence many CCD imaging systems use an optical low-pass filter to eliminate the IR components of the incident illumination.

These limits may be extended up to 30% by various design and manufacturing techniques on a custom application basis.

Fairchild Weston-CCD has also developed prototype sensors using platinum silicide Schottky barrier technology which extend IR performance out to 5.5μm.

Ultraviolet Performance
The newest CCD designs (CCD134, 145, 181, etc.) have at least twice the quantum efficiency in the near-UV (300-400nm) as older designs. Quantum efficiencies of >50% at 400nm are typical.

This improvement can be applied to many current devices and to custom designs on a custom application basis.

Very High Data Rates The standard product assortment of line-scan image sensors include data rate capabilities exceeding 20 MHz sample rate. Since the data rate is limited by the output amplifier, some of our devices—using the charge output directly—have been operated at over 60 MHz.

Even higher effective data rates are possible in custom designs using multiple outputs where each output could run at up to 15-20 MHz and the total data rate is a function of the number of outputs employed.

Long Linear Arrays The longest device currently available in the standard product line is the CCD151 linear sensor—3456 pixels in a row. Longer contiguous lines of pixels can be provided on a custom basis up to the limits of the 4-inch wafer.

Even longer linear configurations can be achieved by staggering devices to produce the desired number of pixels. Various optical techniques, such as beam-splitters, can be employed to create a longer sense line.

The ends of two linear arrays or multiple linear arrays may be joined to achieve a very long sense area, but a few pixels will be lost at the butt joint itself. Fiber bundles can be used in a lens-less system for ultra long, high resolution sense lines with no loss, however.

Fiber Optics Face Plates Most Fairchild Weston CCD linear and area sensors can be fitted with a fiber optics face plate to efficiently couple the optical signal from an image intensifier or other component. (The CCD222 TV image sensor is currently available with such an option.)

Special packaging Some applications require special packages to match unique environments. Fairchild engineers are available to determine the range of possibilities.

Special Screenings Military and space programs often require special screening to meet MIL SPEC 883C or similar applications. Fairchild Weston CCD Imaging Division has considerable experience in screening devices to these specifications.

Other Custom Capabilities Fairchild Weston's CCD staff engineers can provide assistance in other areas as well—AR coated windows, cryogenic temperature operation, special window materials, IR-coated windows, etc. We invite you to consult our experienced sales and application people to discuss a particular requirement.

Linear Imaging Sensor Selection Guide

LINEAR IMAGE SENSOR SELECTION GUIDE

CCD Device	Number of Pixels	Pixel Size (μm)	Pixel Pitch (μm)	Maximum Data Rate (Mhz)	SPECIAL FEATURES: Very Low Light Levels	Anti-Blooming & Int. Control	Correlated Double Samp.	Extended Blue Response
		13 × 17	13				✔	
		13 × 13		20.0				
		13 × 13	13					
		13 × 13	13					✔
+		13 × 13					✔	
		10 × 13	10	2.0			✔	
		13 × 13	13	5.0		✔	✔	✔
		13 × 13	13				✔	
		10 × 10	10		✔		✔	✔
							✔	

+ Limited demand product CCD123 is recommended for new designs.

Number of Pixels:
The desired system resolution determines how many pixels are needed on the CCD. Devices are available with up to 3456 pixels (CCD151). Should more pixels be desired, two or more CCDs may be optically butted.

Data Rate:
The typical maximum data rate for f_{data} is given. Devices with data rates of 10MHz or greater have two outputs —one for even numbered pixels and one for odd The minimum exposure time for a device with N pixels is about $(20 + N)/f_{DATA}$.

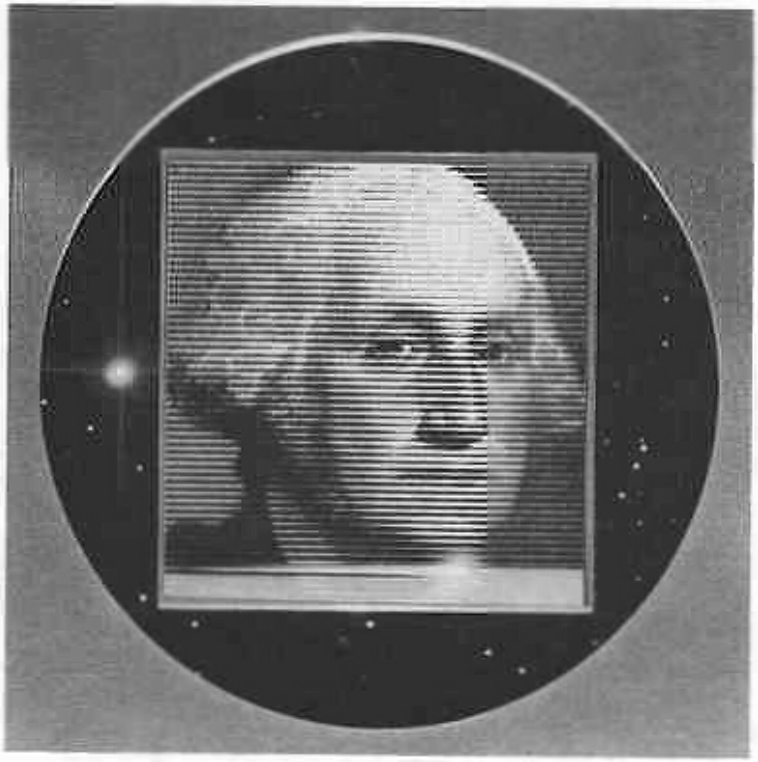
Pixel Size and Spacing:
The system optical aperture size and sensitivity desired determine which pixel size is necessary.

Sensitivity at Very Low Light Levels:
These devices are ideal for rapidly detecting changes in illumination at the lowest illumination levels. They are optimized for minimal retention of signal charge in photosites.

Anti-Blooming/Integration Control:
For applications in which the dynamic range of the scene occasionally exceeds the dynamic range of the device, anti-blooming is recommended. This feature prevents extremely bright sections of the image from causing overflow of the CCD shift register. Integration control allows the optical signal integration time to be less than the exposure time. See application notes for details.

Extended Blue Response:
Devices with extended blue response have 50-100% greater responsivity at 400nm than previous devices. These devices are recommended for applications in which much of the image information is in the blue region.

Correlated Double Sampling (CDS) Compatible:
Correlated double sampling is a technique for increasing the signal-to-noise ratio of a CCD-A/D system. Most Fairchild CCDs can use CDS. CDS can only be used with the internal Sample and Hold disabled and externally supplied reset clock. See application notes for details.



Linear CCD Sensors

Fairchild Weston's advanced buried-channel CCD technology allows line scan sensors to offer excellent charge-transfer efficiency at high data rates with low noise, high S/N ratios and relatively small die sizes.

Line scan sensors are useful in document scanning systems for optical character recognition (OCR) and facsimile data acquisition as well as for measurement and inspection of industrial components, for printed circuit and semiconductor die or wafer inspection and for similar non-contact measurement applications.

FAIRCHILD WESTON

CCD IMAGING DIVISION

CCD 111
256-Element
Line Scan Image Sensor

FEATURES

- **256 × 1 photosite array**
- **13μm × 17μm photosites on 13μm pitch**
- **Dynamic range typical: 7000:1**
- **On-chip video and compensation amplifiers**
- **Low power requirements**
- **All operating voltages 15V and under**
- **Low noise equivalent exposure**
- **Dimensionally precise photosite spacing**

DESCRIPTION

The CCD111 is a monolithic 256-element line image sensor. The device is designed for optical character recognition and other imaging applications that require high sensitivity and high speed. The CCD111 is pin-for-pin compatible with and a functional replacement for the CCD110F.

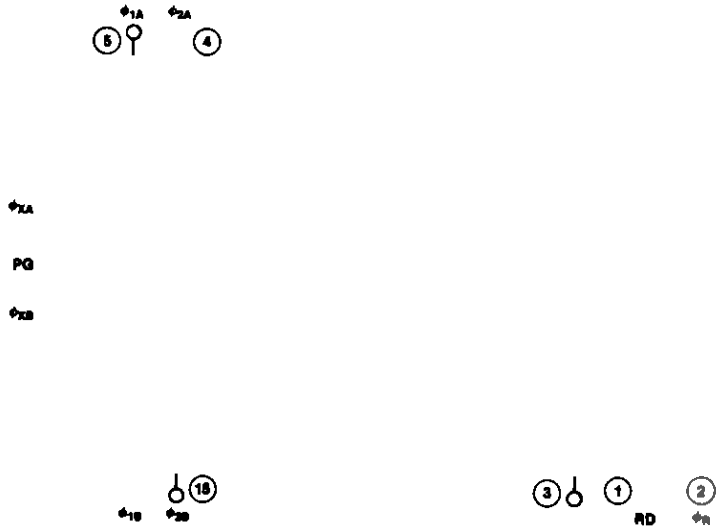
The cell size is 13 μm (0.51 mils) by 17 μm (0.67 mils) on 13 μm (0.51 mils) centers. The device is manufactured using Fairchild Weston advanced charge-coupled device n-channel Isoplanar buried-channel technology.

PIN NAME	DESCRIPTION
PG	Photogate
ϕXA, ϕXB	Transfer Clocks
ϕ1A, ϕ2A	Transport Clocks
ϕ1B, ϕ2B	
OG	Output Gate
OS	Output Source
OD	Output Drain
CS	Compensation Source
ϕR	Reset Clock
RD	Reset Drain
TP	Test Point
V_{SS}	Substrate (ground)

PIN CONNECTION DIAGRAM (TOP VIEW)

Fairchild Weston Systems, Inc. CCD Imaging Division
810 W. Maude Ave., Sunnyvale, California 94086
(408) 720-7600, TWX 910-373-2110

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The CCD111 consists of the following functional elements illustrated in the Block Diagram:

Image Sensor Elements — A row of 256 image sensor elements separated by a diffused channel stop and covered by a silicon photogate. Image photons pass through the transparent polycrystalline silicon photogate and are absorbed in the single crystal silicon creating hole-electron pairs. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated in each photosite is a linear function of the incident illumination intensity and the integration period. The output signal will vary in an analog manner from a thermally generated background level at zero illumination to a maximum at saturation under bright illumination.

Two Transfer Gates — Gate structures adjacent to the row of image sensor elements. The charge packets accumulated in the image sensor elements are transferred out via the transfer gates to the transport registers whenever the transfer gate voltages go HIGH. Alternate charge packets are transferred to the left and right transport registers. The transfer gates also control the integration time for the sensing elements.

Two 130-bit Analog Transport Shift Registers — One on each side of the line of image sensor elements and separated from it by a transfer gate. The two registers, called the transport registers, are used to move the light generated charge packets delivered by the transfer gates serially to the charge detector/amplifier. The complementary phase relationship of the last elements of the two transport registers provides for alternate delivery of charge packets to establish the original serial sequence of the line of video in the output circuit.

A Gated Charge Detector/Amplifier — Charge packets are transported to a precharged diode whose potential changes linearly in response to the quantity of the signal charge delivered. This potential is applied to the gate of the output n-channel MOS transistor producing a signal at the output OS. A reset transistor is driven by the reset clock (ϕ_R) and recharges the charge detector diode capacitance before the arrival of each new signal charge packet from the transport registers.

DEFINITION OF TERMS

Charge-Coupled Device — A charge-coupled device is a semiconductor device in which finite isolated charge packets are transported from one position in the semiconductor to an adjacent position by sequential clocking of an array of gates. The charge packets are minority carriers with respect to the semiconductor substrate.

Transfer Clocks ϕ_{XA}, ϕ_{XB} — The voltage waveforms applied to the transfer gates to move the accumulated charge from the image sensor elements to the CCD transport registers.

Transport Clocks ϕ_{1A}, ϕ_{2A}, ϕ_{1B}, ϕ_{2B} — The two sets of 2-phase waveforms applied to the gates of the transport registers to move the charge packets received from the image sensor elements to the gated charge detector/amplifier.

Gated Charge Detector/Amplifier — The output circuit of the CCD111 that receives the charge packets from the transport registers and provides a signal voltage proportional to the size of each charge packet received. Before each new charge packet is sensed, a reset clock returns the charge detector voltage to a fixed level.

Reset Clock ϕ_R — The voltage waveform required to reset the voltage on the charge detector.

Dynamic Range — The saturation exposure divided by the rms noise equivalent exposure. (This does not take into account dark signal components.) Dynamic range is sometimes defined in terms of peak-to-peak noise. To compare the two definitions a factor of four to six is generally appropriate in that peak-to-peak noise is approximately equal to four to six times rms noise.

RMS Noise Equivalent Exposure — The exposure level that gives an output signal equal to the rms noise level at the output in the dark.

Saturation Exposure — The minimum exposure level that will produce a saturation output signal. Exposure is equal to the irradiance times the photosite integration time.

Charge Transfer Efficiency — Percentage of valid charge information that is transferred between each successive stage of the transport registers.

Responsivity — The output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure.

Total Photoresponse Non-uniformity — The difference of the response levels of the most and least sensitive element under uniform illumination. Measurement of PRNU excludes first and last elements. (See accompanying photos for details of definition.)

Dark Signal — The output signal in the dark caused by thermally generated electrons that is a linear function of the integration time and highly sensitive to temperature. (See accompanying photos for details of definition.)

Saturation Output Voltage — The maximum useable signal output voltage. Charge transfer efficiency decreases sharply when the saturation output voltage is exceeded.

Integration Time — The time interval between the falling edges of any two transfer pulses ϕ_{XA} or ϕ_{XB} as shown in the timing diagram. The integration time is the time allowed for the photosites to collect charge.

Pixel — A picture element (photosite).

Peripheral Response — The output signal caused by light-generated charge that is collected by the transport registers (instead of the the photosites). The primary cause of peripheral response on CCD111A/B devices manufactured after date code 81-01 is optical crosstalk from the photosites to the shift registers.

Major Differences Between the CCD111A and CCD111B
Both the CCD111A and the CCD111B have the same responsivity to visible light (400-700nm). The peripheral differences are as follows:

The CCD111A is intended for use in applications where very low dark signal and high responsivity to very near-infrared (700-900nm) light are needed, and where peripheral response is not critical.

The CCD111B is selected for use in applications where standard responsivity to very near-infrared (700-900nm) light and standard dark signal are acceptable and where peripheral response needs to be minimized.

It is not recommended that either part be used with illumination containing wavelengths greater than 900nm (near-infrared). If use of such a light source (unfiltered tungsten, for example) is unavoidable, the CCD111B will generally provide the user with more satisfactory results. The table on performance characteristics provides more information.

Absolute Maximum Ratings

Storage Temperature	-25°C to 100°C
Operating Temperature	-25°C to 55°C
Pins 2, 3, 4, 5, 6, 7, 10, 12, 13, 14, 15	-0.3V to 15V
Pins 1, 8, 11, 16	-0.3V to 18V
Pins 17, 18	output, no voltage applied
Pin 9	0V

TEST LOAD CONFIGURATION

DC CHARACTERISTICS: $T_c = 25°C$ (Note 1)

SYMBOL	CHARACTERISTIC	LIMITS TYP	UNIT	CONDITION
		15.0		

CLOCK CHARACTERISTICS: $T_c = 25°C$ (Note 1)

AC CHARACTERISTICS: $T_c = 25°C$, $f_{\phi R} = 1.0MHz$, $t_{int} = 320\ \mu s$, $t_{transport} = 259\ \mu s$, Light Source = 2854° K + filters as specified. All operating voltages nominal specified values. (Note 1) All tests done using "Test Load Configuration."

SYMBOL	PARAMETER	RANGE MIN	RANGE TYP	RANGE MAX	UNIT	CONDITION
DR	Dynamic Range					
	(relative to rms noise)		7000:1			Note 7
	(relative to peak-to-peak noise)		1400:1			
NEE	RMS Noise Equivalent Exposure		2×10^{-2}		$\mu J/cm^2$	
SE	Saturation Exposure		0.5		$\mu J/cm^2$	
CTE	Charge Transfer Efficiency	.99990	.99999			Note 8
P	Power Dissipation		100		mW	$V_{OD} = 15V$
Z	Output Impedance		1000		Ω	
N	RMS Noise		100		μV	
	Peak-to-Peak Noise		500		μV	

PERFORMANCE CHARACTERISTICS: T_p = 25°C, $f_{\phi R}$ = 1.0MHz, t_{int} = 320 µs, $t_{transport}$ = 259 µs, Light Source = 2854°K + filters as specified. All operating voltages nominal specified values (Note 1)

		<1
		<1
		<1
		<2
		3
25		4

NOTES:

1. T_C is defined as the package temperature, measured on the back surface of the ceramic header.
2. Negative transients on any clock pin going below 0.0V may cause charge injection that results in an increase in the apparent Dark Signal.
3. $V_{\phi RH}$ should track V_{RD}.

ι $f_{\phi 1B}$, $f_{\phi 2A}$, $f_{\phi 2B}$)

k-to-Peak (temporal) Noise."

ɜ for every 5°C increase in T_C. The shift register component is also inversely

11 Single-pixel Dark Signal non-uniformity (SPDSNU) approximately doubles for every 6°C increase in T_C. They are also directly proportional to the integration time t_{int}.

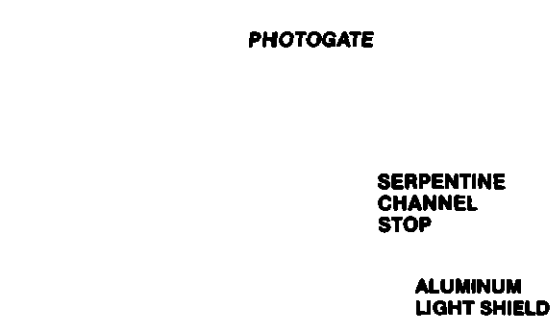
ı SPDSNU.

iadiant Energy measured over the 350 nm - 1200 nm band." The device will not e radiant energy from a 2854° K source is at λ > 1200 nm. For the unfiltered 2854° K -0.3X of the responsivity values for light measured over 350 nm < λ < 1200 nm. Band Hot Mirror" (Optical Coating Labs, Inc., Santa Rosa, California) and one 2.0 a) filter in series. The "900 nm cutoff" filter is available on special order; consult ı for the two cutoff filters and Spectral Energy Distribution curves for these filters ' section of this data sheet. It should be noted that the "2854° K + 700 nm cutoff"

ll PRNU measurements exclude the outputs from the first and last photoelements ɜ array divided by the diameter of the lens aperature. As f number increases, the lons to dominate and increase the PRNU. A lower f number (f≤5) results in less

17. See test load configuration.

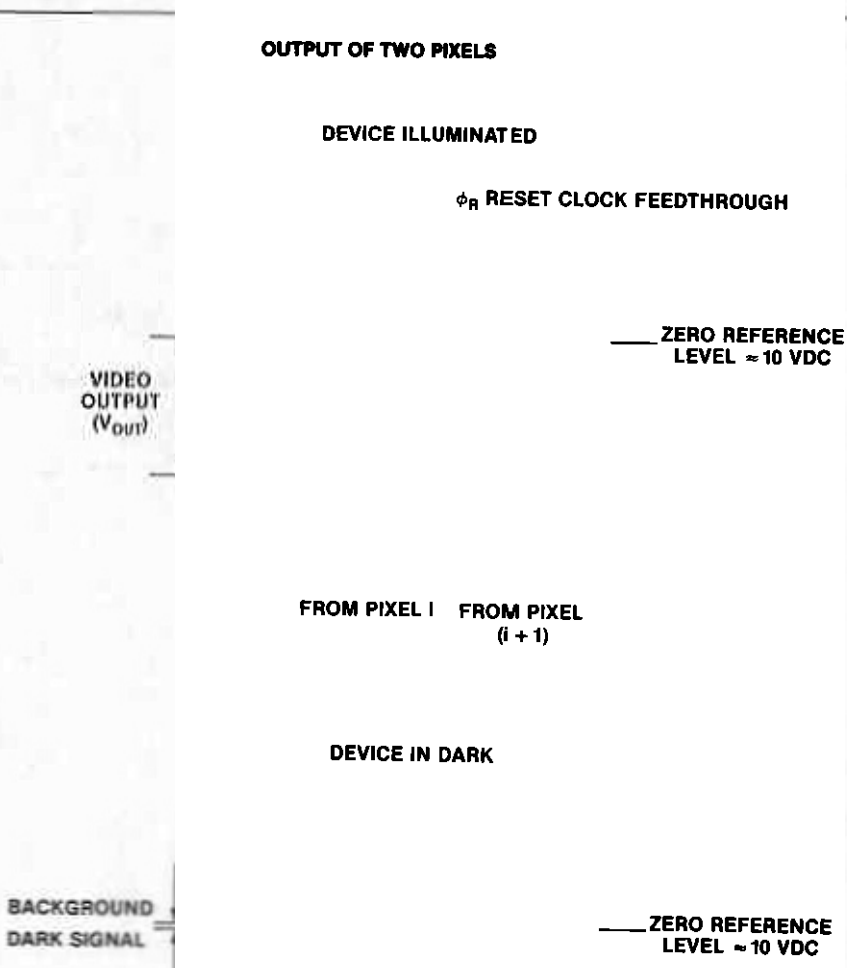
PHOTOELEMENT DIMENSIONS



ALL DIMENSIONS ARE TYPICAL VALUES.

OUTPUT WITH UNIFORM ILLUMINATION

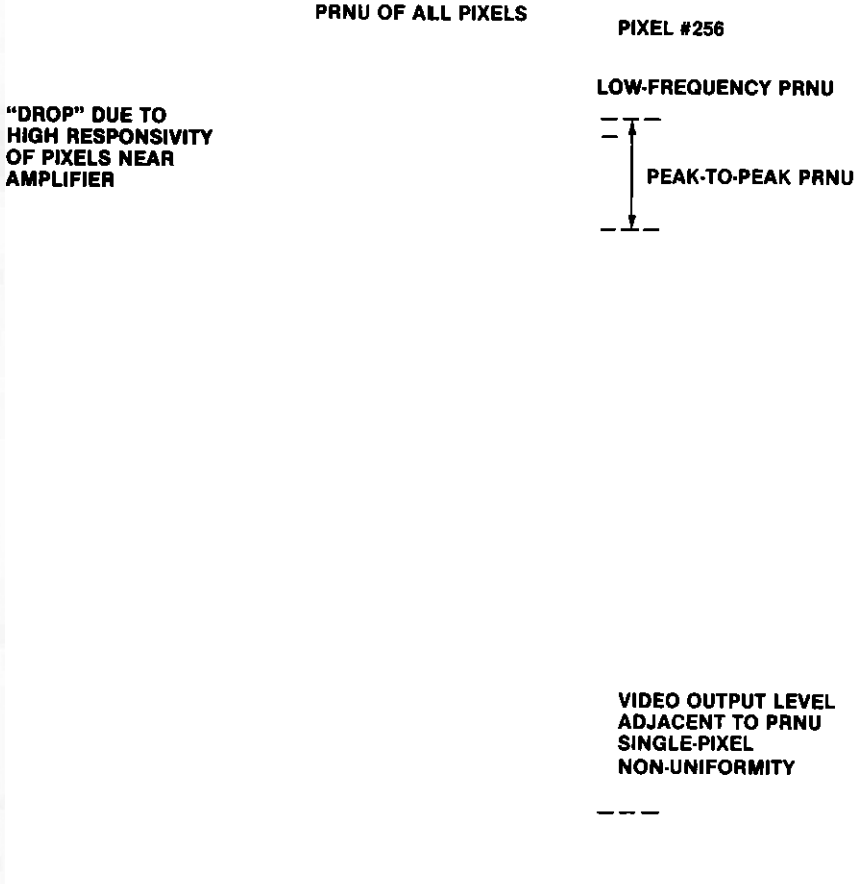
TEST CONDITIONS: $T_C + 25°C$, $t_{int} = 640\ \mu s$, $f_\phi = 512$ kHz, "typ" voltage inputs, 2854°K + 700 nm cutoff filter set. (Half standard test speeds for clearer photos.)



TEST CONDITIONS: $T_C + 25°C$, t_{int} = 640 μs, f_ϕ = 512 kHz, "typ" voltage inputs, 2854°K + 700 nm cutoff filter set. (Half standard test speeds for clearer photos.)

PHOTORESPONSE NON-UNIFORMITY

MEASURED AT V_{OUT} = 350 mV; ALL PRNU COMPONENTS EXCLUDE PIXELS #1 AND #256.



TEST CONDITIONS: T_C = +25°C, t_{int} = 320 μs, $f_{\phi R}$ = 1.0 MHz, 2854°K + 700 nm cutoff filter set, "typ" voltage inputs.

DC + LOW FREQUENCY DARK SIGNAL

AT t_{int} = 640μs:

$t_{integration}$

ZERO REFERENCE ≈ 10 VDC

DC-COMPONENT

SHIFT-REGISTER COMPONENT

LOW-FREQUENCY COMPONENT

REGISTER IMBALANCE

AT t_{int} = 900μs, OTHER INPUTS SAME AS ABOVE:

DC-COMPONENT

LOW-FREQUENCY COMPONENT

TEST CONDITIONS: T_C = +25°C, t_{int} = (as above), $f_{\phi R}$ = 512 kHz, "typ" voltage inputs, (Half standard test speeds for clearer photos.)

SINGLE-PIXEL DARK SIGNAL NON-UNIFORMITY

DC + LOW FREQUENCY

ZERO REFERENCE LEVEL
≈ 10 VDC

TEST CONDITIONS: T_C = +25° C, t_{int} = 2.560ms, $f_{\phi R}$ = 128 kHz, "typ" voltage inputs. (One-eight standard test speeds to emphasize Dark Signal.)

PERIPHERAL RESPONSE

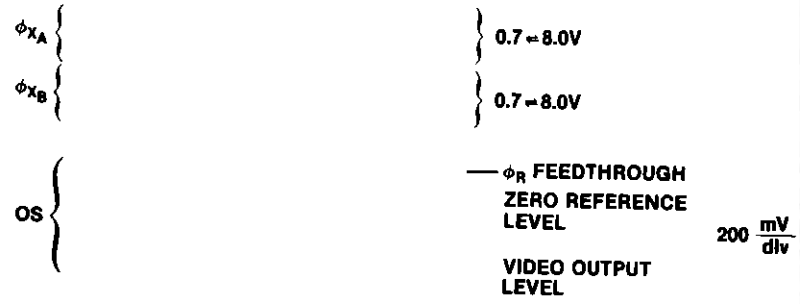
ZERO REFERENCE LEVEL
≈ 10 VDC

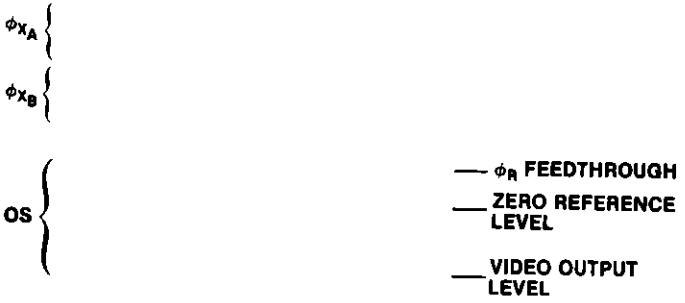
PERIPHERAL RESPONSE

– – –VIDEO OUTPUT LEVEL

TEST CONDITIONS: T_C = +25° C, t_{int} = 640 μs, $f_{\phi R}$ = 510 kHz, "typ" voltage inputs, 2854° K + 700 nm cutoff filter set. (Half standard test speeds for clearer photos.)

φX (TRANSFER CLOCK) COUPLING INTO OS (OUTPUT)





ϕ_{X_A} CLOCK COUPLING ϕ_{X_B} CLOCK COUPLING

DEVICE CARE AND OPERATION

Charge Injection: Every input pin has a gate protection structure that includes a diode from the input to the (grounded) substrate V_{SS}. The diode is reverse-biased during normal operation ($V_{IN} > V_{SS}$). Negative (transient) input voltages ($V_{IN} < V_{SS}$) will forward-bias the diode, injecting electrons into the bulk silicon of the CCD chip.

If sufficient charge is injected, it will accumulate in the transport register(s) and/or the photosites near the injecting gate protection structure(s). Injected charge which accumulates in the photosites will typically result in an apparent bell-shaped increases in Dark Signal (≈ 20-200 pixels wide) near the injecting gate protection structure. Injected charge which accumulates in a transport register will result in an apparent uniform increase in that register's low frequency dark signal, creating a noticeable increase in the apparent Register Imbalance ("odd/even") of the Dark Signal.

The susceptibility to charge injection sufficient to increase the DC and Low Frequency Dark Signal varies significantly from device to device. It is not possible to select devices with "low" susceptibility. However, devices with low Dark Signal are typically more susceptible than devices with high Dark Signal.

Sufficient charge to appear as increased DC and Low Frequency Dark Signal may be injected by negative transient voltages < 4 ns long. Since these transients cannot be detected by oscilloscopes with less than 250-500 MHz bandwidth, a system which appears to be free from negative transients on a 200 MHz scope may still be prone to charge injection. The recommended method to eliminate charge injection is the following diode clipper circuit with suitable damping resistors between the clock drivers and the CCD111:

+5 TO +

Since $C_{\phi R} << C_{\phi 1} \approx C_{\phi 2} \approx (3 \cdot C_{\phi X})$, the damping resistors should be selected so that $R_{\phi R} >> R_{\phi 1} = R_{\phi 2} \approx (1/3 \cdot R_{\phi X})$.

It is also important to note in design and applications considerations that the devices are very sensitive to thermal conditions. The DC and Low Frequency Dark Signal approximately doubles for every 5° C temperature increase and Dark Signal Non-Uniformities approximately double for every 8° C increase. The devices may be cooled to achieve very long integration times and very low light level capability.

Glass may be cleaned by saturating a cotton swab in alcohol and lightly wiping the surface. Rinse off the alcohol with delonized water. Allow the glass to dry, preferably by blowing with filtered dry N_2 or air.

TYPICAL PERFORMANCE CURVES

TYPICAL SPECTRAL RESPONSE

RESPONSIVITY V/μJcm⁻²

— — MIN AND MAX CCD111A
— — MIN AND MAX CCD111B

OUTPUT SIGNAL LEVEL VERSUS INTEGRATION TIME 2854 K TUNGSTEN SOURCE WITH BG-38 AND WBHM FILTER

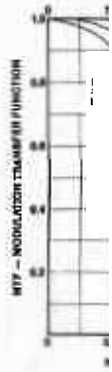
≈ 100%

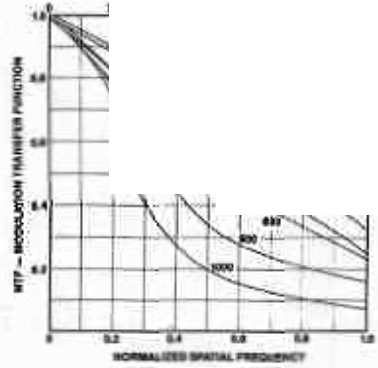
t_{int} - INTEGRATION TIME (ms)

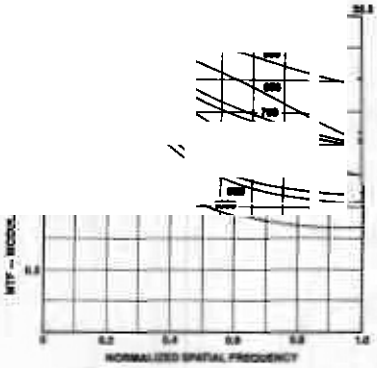
TYPICAL PERFORMANCE CURVES (cont'd)

DARK SIGNAL NON-UNIFORMITY
VERSUS INTEGRATION TIME

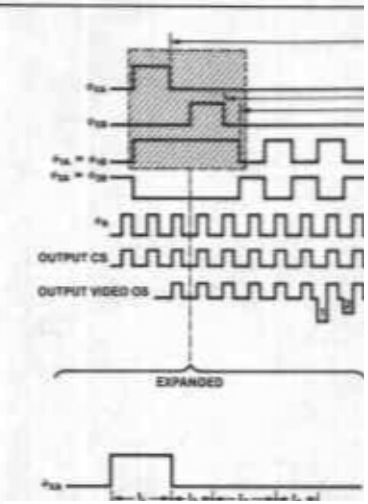
RELATIVE IRRADIANCE
VERSUS WAVELENGTH

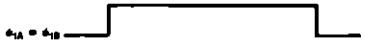






TIMING DIAGRAM DRIVE





$\phi_{2A} = \phi_{2B}$

ϕ_R

Timing requirements for transfer Gate Pulses ϕ_{XA}, ϕ_{XB}
No requirement for t_2 - ϕ_{2A} may be tied to ϕ_{XB}

$t_1 = t_3 > 0.8\mu s$
$t_4 > 0.1\mu s$

$20ns < (t_r = t_f) < 80ns$

Timing requirements for Reset Pulse ϕ_R

$t_r = t_f < 20ns$
$0.2(t_{cR}) < t_{\phi R} < 0.3(t_{cR})$

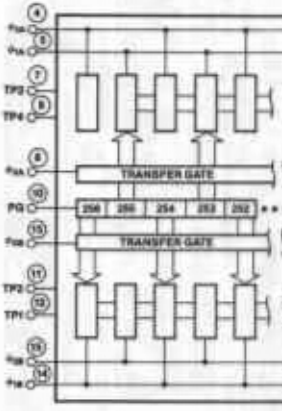
Timing requirements for ϕ_{1A}, ϕ_{1B}

$20ns < (t_r = t_f) < 100ns$

ϕ_1 and ϕ_2 clocks may not both be < 3.5V simultaneously.

VIDEO DATA VALID
FROM REGISTER A

CIRCUIT DIAGRAM



○ = Pin Numbers

ORDER INFORMATION

It is important to note that two different selections of the CCD111 are being offered for applications that differ in the wavelength of light used for imaging. Please refer to the section "Major Differences Between the CCD111A and CCD111B" on page 13 before placing an order.

To order the CCD111, please follow the ordering codes listed in the table below:

CCD111A 256 × 1 Line Image Sensor

CCD111B 256 × 1 Line Image Sensor

A printed circuit board is available which includes all the necessary clocks, logic drivers, and video amplifiers to operate the CCD111. The board is fully assembled and tested and requires ±15V and +5V supplies for operation. The printed circuit board order code is I-SCAN.

CCD111DC Package Outline
18-Pin Dual In-Line Ceramic Package

0.048 (1.22)
TOP OF DIE
TO TOP OF COVER

FAIRCHILD WESTON

CCD IMAGING DIVISION

CCD122
1728-Element
Linear Image Sensor

FEATURES

- **1728 × 1 photosite array**
- **13μm × 13μm photosites on 13μm pitch**
- **Low dark signal**
- **High responsivity**
- **On-chip clock drivers**
- **Dynamic range typical: 5500:1**
- **Over 1V peak-to-peak output**
- **Dark and white references contained in a sampled-and-held output**
- **Special selections available — consult factory.**

DESCRIPTION

The CCD122 is a monotlithic 1728-element linear image sensor, designed for page scanning applications including facsimile, optical character recognition and other imaging applications which require high resolution and high sensitivity.

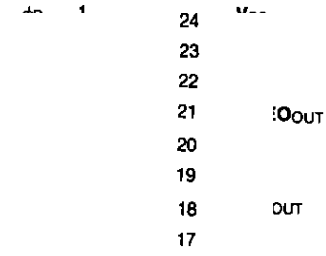
The 1728 sensing elements of the CCD122 provide a 200-line per inch resolution across an 8-1/2 inch page adopted as an international facsimile standard.

The CCD122 also incorporates on-chip clock driver circuitry.

The photoelement size is 13 μm (0.51 mils) by 13 μm (0.51 mils) on 13 μm (0.51 mils) centers. The devices are manufactured using Fairchild Weston advanced charge-coupled device n-channel Isoplanar buried-channel technology.

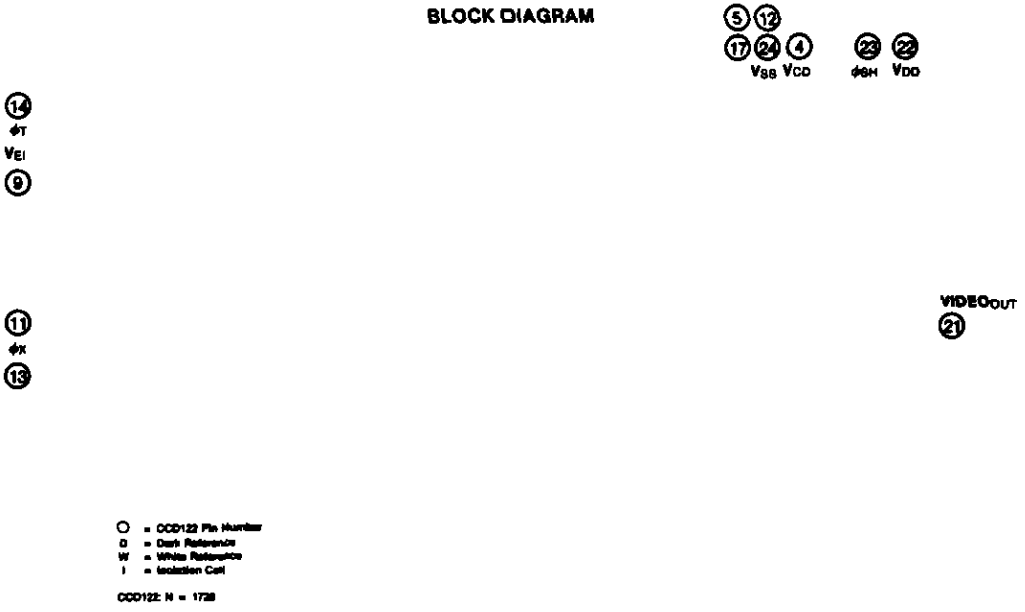
PIN NAME	DESCRIPTION
V_{PG}	Photogate

PIN CONNECTION DIAGRAM (TOP VIEW)



Fairchild Weston Systems, Inc. CCD Imaging Division
810 W. Maude Ave., Sunnyvale, California 94086
(408) 720-7600, TWX 910-373-2110

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Image Sensor Elements — A line of 1728 image sensor elements separated by diffused channel stops and covered by a silicon dioxide surface passivation layer. Image photons pass through the transparent silicon dioxide layer and are absorbed in the single crystal silicon creating hole-electron pairs. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated in each photosite is a linear function of the incident illumination intensity and the integration period. The output signal will vary in an analog manner from a thermally generated noise background at zero illumination to a maximum at saturation under bright illumination.

Transfer Gate — Gate structure adjacent to the line of image sensor elements. The charge-packets accumulated in the image sensor elements are transferred out via the transfer gate to the transport registers whenever the transfer gate voltage goes HIGH. Alternate charge-packets are transferred to the analog transport shift registers. The transfer gate also controls the exposure time for the sensing elements and permits entry of charge to the End-Of-Scan (EOS) shift registers creating the end-of-scan waveform.

Four 879-Bit Analog Shift Registers — Two on each side of the line of image sensor elements and separated from it by the transfer gate. The two inside registers, called the transport shift registers, are used to move the image generated charge-packets delivered by the transfer gate serially to the charge-detector/amplifier. The complementary phase relationship of the last elements of the two transport shift registers provides for alternate delivery of charge-packets to establish the original serial sequence of the line of video in the output circuit. The outer two registers serve to deliver the end-of-scan waveform and reduce peripheral electron noise in the inner shift registers.

Gated Charge-Detector/Amplifier — Charge-packets are transported to a precharged diode whose potential changes linearly in response to the quantity of the signal charge delivered. This potential is applied to the gate of an n-channel MOS transistor producing a signal which passes through the sample-and-hold gate to the output at $VIDEO_{OUT}$. The sample-and-hold gate is a switching MOS transistor in the output amplifier that allows the output to be delivered as a sampled-and-held waveform. A reset transistor is driven by the Reset Clock (ϕ_R) and recharges the charge-detector diode capacitance before the arrival of each new signal charge-packet from the transport registers.

Clock Driver Circuitry — Allows the CCD122 to be operated using only three external clocks, (1) a Reset Clock signal which controls the integrated output signal amplifier, (2) a square wave Transport Clock which operates at half the reset clock frequency and controls the readout rate of video data from the sensor, and (3) a Transfer Clock pulse which controls exposure time of the sensor. The external clocks should be able to suppy TTL level power.

Dark and White Reference Circuitry — Four additional sensing elements at both ends of the 1728 array are covered by opaque metalization. They provide a dark (no illumination) signal reference which is delivered at both ends of the line of video output representing the illuminated 1728 sensor elements (labelled "D" in the block diagram). Also included at one end of the 1728 sense element array is a white signal reference level generator which likewise provides a reference in the output signal (labelled "W" in the block diagram). These reference levels are useful as inputs to external DC restoration and/or automatic gain control circuitry.

DEFINITION OF TERMS:

Charge-Coupled Device — A charge-coupled device is a semiconductor device in which finite isolated charge-packets are transported from one position in the semiconductor to an adjacent position by sequential clocking of an array of gates. The charge-packets are minority carriers with respect to the semiconductor substrate.

Transfer Clock ϕ_X — The voltage waveform applied to the transfer gate to move the accumulated charge from the image sensor elements to the CCD transport shift registers.

Transport Clock ϕ_T — The clock applied to the gates of the CCD transport shift registers to move the charge-packets received from the image sensor elements to the gated charge-detector/ amplifier.

Reset Clock ϕ_R — The voltage waveform required to reset the voltage on the charge-detector.

Sample-and-Hold Clock ϕ_{SH} — An internally supplied voltage waveform applied to the sample-and-hold gate in the amplifier to create a continuous sampled video signal at the output. The sample-and-hold feature can be defeated by connecting ϕ_{SH} to V_{DD}.

Dark Reference — Video output level generated from sensing elements covered with opaque metalization providing a reference voltage equivalent to device operation in the dark. Permits use of external dc restoration circuitry.

Isolation Cell — A site on-chip producing an element in the video output that serves as a buffer between valid video data and dark and white reference signals. The output from an isolation cell contains no valid video information and should be ignored.

Peak-to-Peak Noise Equivalent Exposure — The exposure level which gives an output signal equal to the peak-to-peak noise level at the output in the dark.

Saturation Exposure — The minimum exposure level that will produce a saturated output signal. Exposure is equal to the light intensity times the photosite integration time.

Charge Transfer Efficiency — Percentage of valid charge information that is transferred between each successive stage of the transport registers.

Responsivity — The output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure level.

Dark Signal — The output signal in the dark caused by thermally generated electrons which is a linear function of integration time and highly sensitive to temperature. (See accompanying photos for details of definition.)

Total Photoresponse Non-Uniformity — The difference of the response levels between the most and least sensitive elements under uniform illumination. (See accompanying photos for details of definition.)

Integration Time — The time interval between the falling edges of any two successive transfer pulses ϕ_X as shown in the timing diagram. The integration time is the time allowed for the photosites to collect charge.

Pixel — Picture element (photosite).

TEST LOAD CONFIGURATION

END-OF-SCAN WAVEFORM

PHOTOELEMENT DIMENSIONS

ABSOLUTE MAXIMUM RATINGS (Above which useful life may be impaired)

Storage Temperature
Operating Temperature

CCD122 Pins 1, 4, 9, 10, 11, 13, 14, 16, 22, 23
Pins 5, 12, 17, 24
Pins 2, 3, 6, 7, 8, 15, 19, 20,
Pins 18, 21

CAUTION NOTE: These devices have limited built-in gate protection. It is recommended that static discharge be controlled and minimized. Care must be taken to avoid shorting pins $VIDEO_{OUT}$ and EOS_{OUT} to V_{SS} or V_{DD} during operation of the device. Shorting these pins temporarily to V_{SS} or V_{DD} may destroy the output amplifiers.

DC CHARA

SYMBO						NDITIONS
		12.0				
	Clock Driver Drain Supply Current		6.9	12.5	mA	
	Output Amplifier Drain Supply Voltage	12.0	13.0	14.0	V	
I_{DD}	utput Amplifier Drain Supply Current		6.9	12.5	mA	
	Photogate Bias Voltage	6.5	7.0	7.5	V	
V_T	DC Electrode Bias Boltage	4.5	5.0	5.5	V	Note 2
V_{EI}	Electrical Input Bias Voltage		11.4		V	Note 3
V_{SS}	Substrate (Ground)		0.0		V	

CHARACTERISTICS: (Note 1)
= 25°C, $f_{\phi R}$ = 0.5 MHz, t_{int} = 10 ms, light source = 2854°K + 3.0 mm thick Corning 1-75 IR-absorbing filter. All nominal specified values. All tests done using "Test Load Configuration."

CHARACTERISTIC

Dynamic Range
(relative to peak-to-peak noise)

CLOCK CHARACTERISTICS: T_P = 25°C (Note 1)

PERFORMANCE CHARACTERISTICS: (Note 1)

T_P = 25°C, $f_{\phi R}$ = 0.5 MHz, t_{int} = 10 ms, light source = 2854°K + 3.0 mm thick Corning 1-75 IR-absorbing filter All voltages nominal specified values.

		CONDITIONS
Photoresponse Non-uniformity		
Peak-to-Peak	mV	Note 16
Peak-to-Peak without Single-Pixel Positive and Negative Pulses	mV	Note 16
Single-pixel Positive Pulses	mV	Note 16
Single-pixel Negative Pulses	mV	Note 16
	mV	Note
		Notes 13, 14
		14
		Notes 13, 15
		Note 17
		Note 18

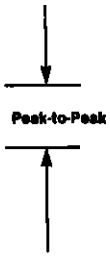
PRNU Measurements taken at 700 mV output level using an f/2.8 lens and excluded the outputs from the first and last elements of the array. The number is defined as the distance from the lens to the array divided by the diameter of the lens aperture. As the f number increases, the resu[illegible] ire highly collimated light causes the package window imperfections to dominate and increase PRNU. A lower f number results in collimated light causing device photosite blemishes to dominate the PRNU.

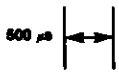
NOTES:

1. TP is defined as the package temperature.
2. VT should be equal to (1/2) $V_{\phi TH}$.
3. VEI is used to generate the end-of-scan output and the white reference output. These two signals can be eliminated by connecting VEI to a voltage level equal to $V_{\phi XH}$ + 5 V.
4. Negative transients on any clock pin going below 0.0 V may cause charge-injection which results in an increase of apparent DS
5. $C_{\phi T}$ ≅ 700 pF
6. $C_{\phi X}$ ≅ 300 pF
7. $C_{\phi R}$ ≅ 5 pF
8. Minimum clock frequency is limited by increase in dark signal.
9. Dynamic range is defined as VSAT/peak-to-peak (temporal) or VSAT/rms noise.
10. 1 μJ/cm² = 0.02 fcs at 2854°K, 1 fcs = 50 μJ/cm² at 2854°K.
11. SE for 2854°K for light without 3.0 mm thick Corning 1-75 IR-absorbing filter is typically 0.8 μJ/cm².
12. CTE is the measurement for a one-stage transfer.
13. See photographs for DS definitions.
14. Dark signal component approximately doubles for every 5°C increase in TP.
15. Each SPDSNU is measured from the DS level adjacent to the base of the SPDSNU. The SPDSNU approximately doubles for every 8°C increase in TP.
16. See photographs for PRNU definitions.
17. Responsivity for 2854°K light source without 3.0 mm thick Corning 1-75 IR-absorbing filter is typically 2 V per μJ/cm².
18. See test load configurations.

PHOTORESPONSE NON-UNIFORMITY PARAMETERS (PRNU)

Zero Reference
Level (≈ +5.5 Vdc)





TEST CONDITIONS
T_P = +25°C, f_{eR} = 0.5 MHz, t_{INT} = 10.0 ms, all voltages nominal spec-sheet values. Illumination: 2854°K source with a 3.0 mm thick Corning 1-75 IR-absorbing filter. PRNU measurements taken at an output voltage of 700 mV.

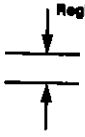
PRNU PARAMETERS (CONTINUED)

nV

nV

Clock Feedthrough

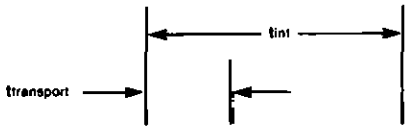
Register Imbalance



TEST CONDITIONS

T_P = +25°C, $f_{\phi R}$ = 0.5 MHz, tint = 10.0 ms, all voltages nominal spec-sheet values. Illumination: 2854°K source with a 3.0 mm thick Corning 1-75 IR-absorbing filter. PRNU measurements taken at an output voltage of 700 mV.

DARK SIGNAL PARAMETERS (DS)



Zero Reference Level
(≅ +5.5 Vdc)

Total Dark Signal

10 mV

Zero Reference Level
(≅ +5.5 Vdc)

10 mV

TEST CONDITIONS
TP ≅ +25°C, f_{eR} = 0.5 MHz, tint = 10.0 ms, all voltages nominal specified values

DS PARAMETERS (CONTINUED)

VIDEO OUTPUT TIMING PHOTOGRAPHS

TEST CONDITIONS

TP = +25°C, fsR = 0.6 MHz, tint = 10 ms, all voltages nominal spec-sheet values. Illumination: 2854°K source with a 3.0 mm thick Corning 1-75 IR-absorbing filter. PRNU measurements taken at an output voltage of 700 mV.

TYPICAL PERFORMANCE CURVES

TYPICAL SPECTRAL RESPONSE

DC AND LOW-FREQUENCY DARK SIGNAL VERSUS INTEGRATION TIME

MODULATION TRANSFER FUNCTIONS FOR NARROW BAND ILLUMINATION SOURCES

SPATIAL FREQUENCY—CYCLES/mm

t_{int} — INTEGRATION TIME — ms

OUTPUT SIGNAL LEVEL VERSUS INTEGRATION TIME 2854°K TUNGSTEN SOURCE WITH CORNING 1-75 FILTER

t_{int} — INTEGRATION TIME — ms

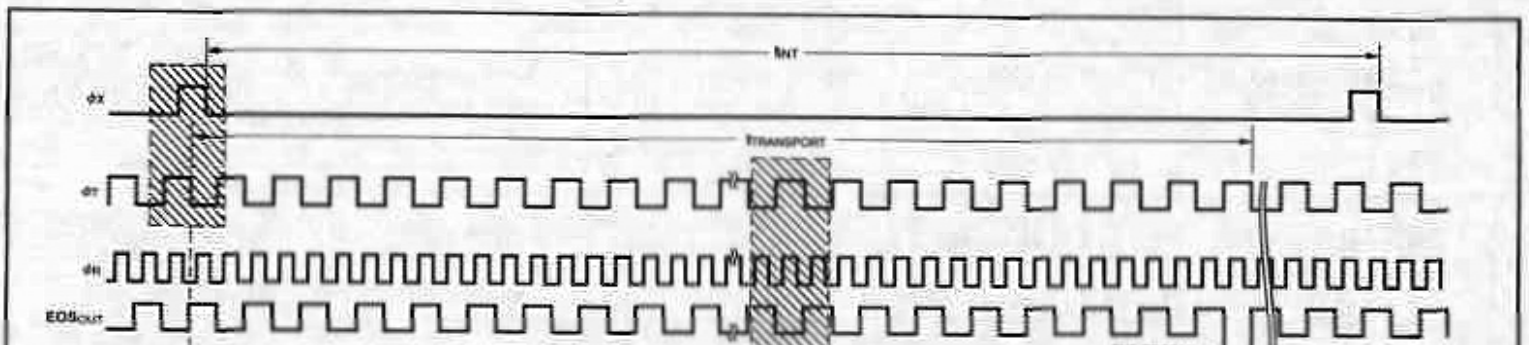
MODULATION TRANSFER FUNCTIONS FOR TWO BROADBAND *ILLUMINATION SOURCES*

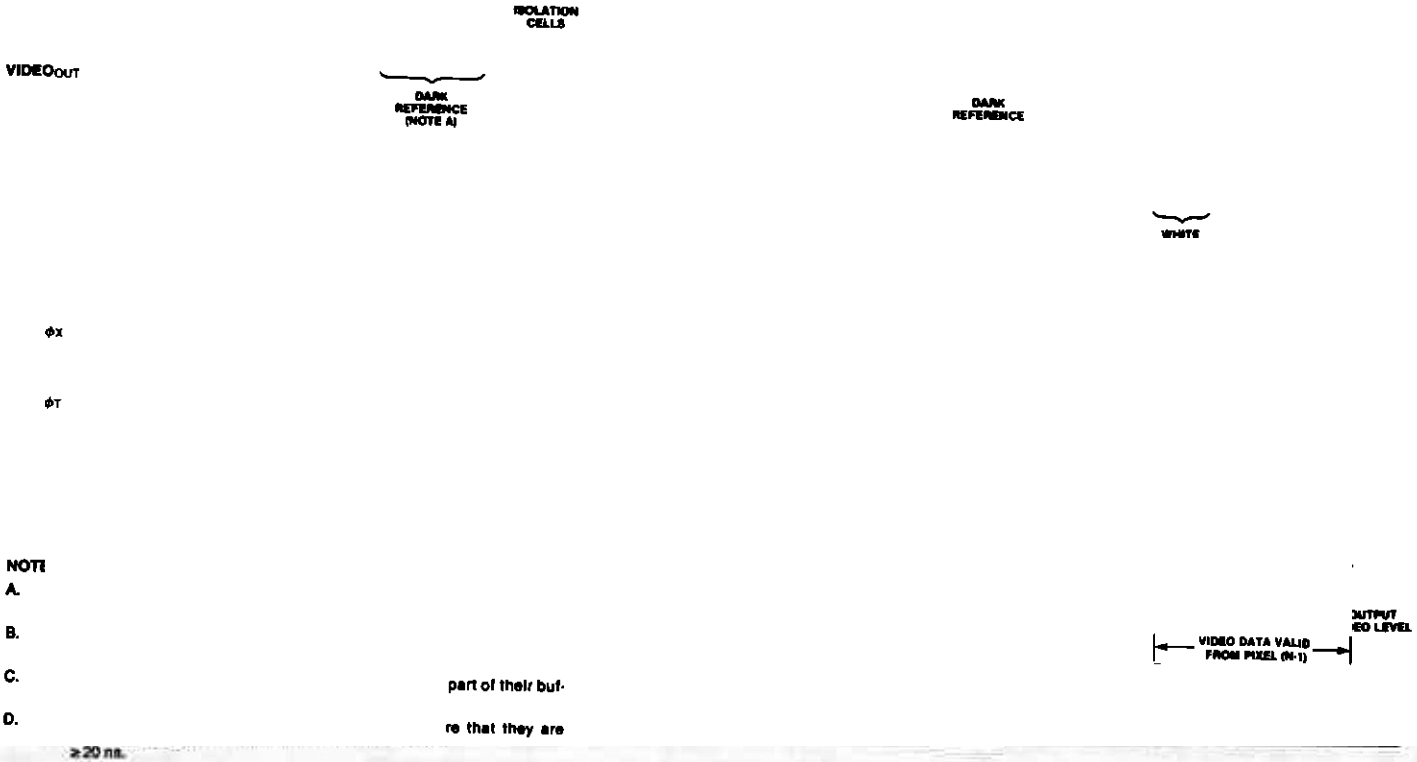
SPATIAL FREQUENCY — CYLES/mm

NORMALIZED SPATIAL FREQUENCY

The Corning 1-75 filter has the following typical transmittance spectral characteristic: >85% at <600 nm, 60% at 700 nm, 30% at 800 nm, 5% at 900 nm and <2% at >1000 nm.

TIMING DIAGRAM DRIVE SIGNALS





NOTE

A.

B.

C. part of their buf-

D. re that they are

≥20 ns.

DEVICE CARE AND OPERATION:

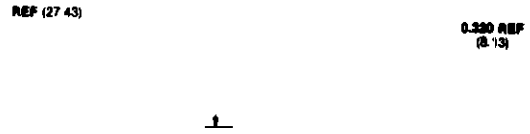
Glass may be cleaned by saturating a cotton swab in alcohol and lightly wiping the surface. Rinse off the alcohol with de-ionized water. Allow the glass to dry preferably by blowing with filtered dry N_2 or air.

It is important to note in design and applications considerations that the devices are very sensitive to thermal conditions. The dark signal DC and low frequency components approximately double for every 5° C temperature increase and single-pixel dark signal non-uniformities approximately double for every 8° C temperature increase. The devices may be cooled to achieve very long integration times and very low light level capability.

ORDER INFORMATION — Order CCD122DC where "D" stands for a ceramic package and "C" for commercial temperature range.

Also available are CCD122DB Design Aid printed circuit boards that include all the necessary clocks, logic drivers and video amplifiers to operate the CCD122DC. The boards are fully assembled and tested and require only one power supply for operation (+15 V). See Page 135.

CCD122DC PACKAGE OUTLINE
24-Pin Dual In-line Ceramic Package



NOTES:
All dimensions in inches (bold) and millimeters (parentheses). Header is black ceramic (Al_2O_3). Window is glass. The amplifier of the device is located near the notched end of the package.

FAIRCHILD WESTON
Schlumberger
CCD IMAGING DIVISION

CCD123
1728-Element Linear Image Sensor

FEATURES

- 1728 × 1 photosite array
- 13μm × 10μm on 10μm pitch.
- Low dark signal.
- High responsivity.
- On-chip clock drivers.
- Dynamic range typical: 5500:1.
- Over 1V peak-to-peak output.
- Dark reference contained in a sampled-and-held output.
- Special selections available — consult factory.

The photo-element size is 10μm (0.39mils) by 13μm (0.5mils) on 10μm (0.39mils) centers. The devices are manufactured using Fairchild Weston advanced charge-coupled device n-channel isoplanar buried-channel technology.

22
21
20
19
18
17
16
15

Fairchild Weston Systems, Inc. CCD Imaging Division
810 W. Maude Ave., Sunnyvale, California 94086
(408) 720-7600, TWX 910-373-2110

Fig. 1 BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION

The CCD123 consists of the following functional elements illustrated in the Block Diagram and circuit diagram (Fig. 1).

Photosites — A row of 1728 image sensor elements separated by a diffused channel stop and covered by a silicon dioxide surface passivation layer. Image photons pass through the transparent silicon creating hole-electron pairs. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated in each photosite is a linear function of the incident illumination intensity and the integration period. The output signal will vary in an analog manner from a thermally generated background level at zero illumination to a maximum at saturation under bright illumination.

Photgate — The photogate structure, located at the edge of the photosites, provides a bias voltage for the photosites.

Transfer Gate — Gate structure adjacent to the line of image sensor elements. The charge-packets accumulated in the image sensor elements are transferred out via the transfer gate to the transport registers whenever the transfer gate voltage goes HIGH. Alternate charge-packets are transferrred to the analog transport shift registers. The transfer gate also controls the exposure time for the sensing elements.

Four 879 Bit Analog Shift Registers — Two on each side of the line of image sensor elements and separated from it by the transfer gate. The two inside registers, called the transport shift registers, are used to move the image generated charge-packets delivered by the transfer gate serially to the charge-detector/amplifier. The complementary phase relationship of the last elements of two transport shift registers provides for alternate delivery of charge-packets to the establish the original serial sequence of the line of video in the output circuit. The outer two registers serve to reduce peripheral electron noise in the inner shift registers.

Gate Charge-Detector/Amplifier — Charge-packets are transported to a precharged diode whose potential changes linearly in response to the quantity of the signal charge delivered. This potential is applied to the gate of an n-channel MOS transistor producing a signal which passes through the sample-and-hold gate to the output at $VIDEO_{OUT}$. The sample-and-hold gate is a switching MOS transistor in the output amplifier that allows the output to be delivered as a sample-and-held waveform. A reset transistor is driven by the Reset Clock (ϕR) and recharges the charge-detector diode capacitance before the arrival of each new signal charge-packet from the transport registers.

Clock Driver Circuitry — Allows the CCD123 to be operated using only three external clocks, (1) a Reset clock signal which controls the integrated output signal amplifier, (2) a square wave Transport Clock which operates at half the reset clock frequency and controls the readout rate of video data from the sensor, and (3) a Transfer Clock pulse which controls exposure time of the sensor. The external clocks should be able to supply TTL level power.

Dark Reference Output — Four additional sensing elements at both ends of the 1728 array are covered by opaque metalization. They provide a dark (no illumination) signal reference which is delivered at both ends of the line of video output representing the illuminated 1728 sensor elements (labelled "D" in the block diagram). The dark reference level is useful as an input to external DC restoration circuitry

DEFINITION OF TERMS:

Transfer Clock ϕX — The voltage waveform applied to the transfer gate to move the accumulated charge from the image sensor elements to the CCD transport shift registers.

Transport Clock ϕT — The clock applied to the gates of the CCD transport shift registers to move the charge-packets received from the image sensor elements to the gated charge-detector/amplifier.

Reset Clock ϕR — The voltage waveform required to reset the voltage on the charge-detector.

Sample-and-Hold Clock ϕSH — An internally supplied voltage waveform applied to the sample-and-hold gate in the amplifier to create a continuous sampled video signal at the output. The sample-and-hold feature can be defeated by connecting Pin V_{SD} to V_{DD}.

Isolation Cell — A site on-chip producing an element in the video output that serves as a buffer between valid video data and dark reference signals. The output from an isolation cell contains no valid video information and should be ignored.

Dynamic Range — The saturation exposure divided by the RMS temporal noise equivalent exposure. Dynamic range is sometimes defined in terms of peak-to-peak noise. To compare the two definitions a factor of four to six is generally appropriate in that peak-to-peak noise is approximately equal to four to six times RMS noise.

RMS Noise Equivalent Exposure — The exposure level that gives an output signal equal to the RMS noise level at the output in the dark.

Saturation Exposure — The minimum exposure level that will provide a saturation output signal. Exposure is equal to the light intensity times the photosite integration time.

Charge Transfer Efficiency — Percentage of valid charge information that is transferred between each successive stage of the transport registers.

Responsivity — The output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure.

Dark Signal — The output signal in the dark caused by thermally generated electrons which is a linear function of integration time and highly sensitive to temperature.

Integration Time — The time interval between the falling edges of any two successive transfer pulses ϕX as shown in the timing diagram. The integration time is the time allowed for the photosites to collect charge.

Total Photoresponse Non-Uniformity — The difference of the response levels of the most and the least sensitive element under uniform illumination. Measurement of PRNU excludes first and last elements.

Saturation Output Voltage — The maximum usable signal output voltage. Charge transfer efficiency decreases sharply when the saturation output voltage is exceeded.

Sample-and-Hold Load Points — Used to reduce charge injection which might be caused by the internal sample and hold clock. Connect 10pf to SH_{L1} and 56pf to SH_{L2}.

Pixel — A picture element (photosite).

Fig. 2 TEST LOAD CONFIGURATION

Fig. 3 PHOTOELEMENT DIMENSIONS

ALL DIMENSIONS ARE TYPICAL VALUES

ABSOLUTE MAXIMUM RATINGS (Above which useful life may be impaired)

Storage Temperature	−25°C to +125°C
Operating Temperature (See "Device Care & Operation")	−25°C to +70°C
CCD123 Pins 1, 4, 10, 11, 13, 14, 16, 22, 23	−0.3V to 18V
Pins 5, 12, 17, 24	0V
Pins 6, 7, 8, 15, 18, 19, 20,	NC
Pins 2, 3, 21	See caution note

CAUTION NOTE: These devices have limited built-in gate protection. It is recommended that static discharge be controlled and minimized. Care must be taken to avoid shorting V_{OUT}, SH_{L1} and SH_{L2} to V_{SS}, V_{SG}, V_{CG} or V_{DD} during operation of these devices. Temporarily shorting this pin may destroy the on-chip clock drivers and/or the output amplifier.

8.0

V_{SS}

V_{SG}

V_{CG}

V_{SD}

$V_{\phi XL}$

$V_{\phi TL}$

$V_{\phi RL}$

f_{data} MAX

AC CHARACTERTISTICS:
T_P = 25°C (Note 1), f_{data} = 0.5 MHz, t_{int} = 10 ms, light source = 2854°K + 2.0mm thick Schott BG-38 and OCLI WBHM filters (Note 7). All operating voltages nominal specified values. All tests done using "Test Load Configuration."

Dynamic Range		
(relative to peak-to-peak noise)		
(relative to rms noise)		
	.00057	$\mu J/cm^2$
	1100	

All PRNU measurements taken at 700 mV output level using an f/5.0 lens and excluded the outputs from the first and last elements of the array. The "f" number is defined as the distance from the lens to the array divided by the diameter of the lens aperture. As the "f" number increases, the resulting more highly collimated light causes the package window imperfections to dominate and increase PRNU. A lower "f" number results in less collimated light causing device photosite blemishes to dominate the PRNU

NOTES:

n good thermal contact with the entire backside of the package.

e injection, which results in an increase of apparent DS

s in T_P
SPDSNU The SPDSNU approximately doubles for every 5-15° C increase in T_P.

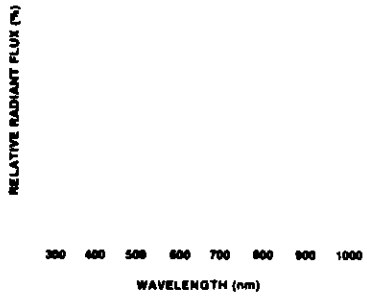
TYPICAL PERFORMANCE CURVES

SINGLE-PIXEL DARK SIGNAL NON-UNIFORMITIES VERSUS INTEGRATION TIME

DC AND LOW-FREQUENCY DARK SIGNAL VERSUS INTEGRATION TIME

TYPICAL SPECTRAL RESPONSE

RELATIVE RADIANT FLUX VS WAVELENGTH



MODULATION TRANSFER FUNCTIONS FOR NARROW BAND ILLUMINATION SOURCES

— — — TYPICAL "DAYLIGHT FLUORESCENT" BULB
— · — 2854°K LIGHT SOURCE +WBHM + 2.0 mm THICK BG-38

MODULATION TRANSFER FUNCTIONS FOR TWO BROADBAND ILLUMINATION SOURCES

TIMING DIAGRAM

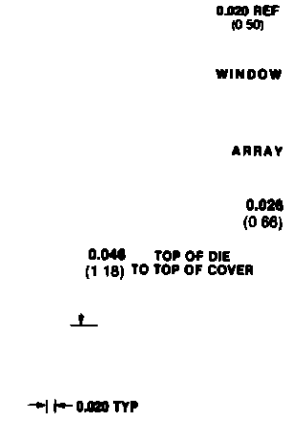
DEVICE CARE AND OPERATION:

Glass may be cleaned by saturating a cotton swab in alcohol and lightly wiping the surface. Rinse off the alcohol with de-ionized water. Allow the glass to dry preferably by blowing with filtered dry N_2 or air.

It is important to note in design and applications considerations that the devices are very sensitive to thermal conditions. The dark signal DC and low frequency components approximately double for every 5° C temperature increase and single-pixel dark signal non-uniformities approximately double for every 8° C temperature increase. The devices may be cooled to achieve very long integration times and very low light level capability.

ORDER INFORMATION – Order CCD123 DC where "D" stands for a ceramic package and "C" for commercial temperature range.

CCD123DC PACKAGE OUTLINE
24-Pin Dual In-line Ceramic Package



NOTES:
All dimensions in inches (bold) and millimeters (parentheses). Header is black ceramic (Al_2O_3). Window is glass. The amplifier of the device is located near the notched end of the package

FAIRCHILD WESTON

CCD IMAGING DIVISION

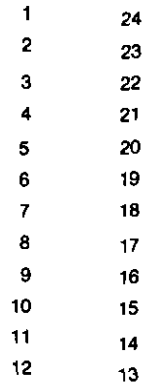
CCD133A
1024-Element High-Speed Linear Image Sensor

FEATURES

- 1024 × 1 photosite array
- 13μm × 13μm photosites on 13μm pitch
- High speed: up to 20 MHz data rate
- Enhanced spectral response
- Low dark signal
- High responsivity
- On-chip clock drivers
- Dynamic range typical: 7500:1
- Over 1 V peak-to-peak outputs
- Dark and white references contained in sample-and-hold outputs
- Special selections available — consult factory.

PIN NAME	DESCRIPTION

PIN CONNECTION DIAGRAM
(TOP VIEW)



Fairchild Weston Systems, Inc. CCD Imaging Division
810 W. Maude Ave., Sunnyvale, California 94086
(408) 720-7600, TWX 910-373-2110

Fig. 1 BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION

The CCD 133A consists of the following functional elements illustrated in the Block Diagram and Circuit Diagram (Fig. 1)

Photosites: A row of 1024 image sensor elements separated by a diffused channel stop and covered by a silicon dioxide surface passivation layer. Image photons pass through the transparent silicon creating hole-electron pairs. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated in each photosite is a linear function of the incident illumination intensity and the integration period. The output signal will vary in an analog manner from a thermally generated background level at zero illumination to a maximum at saturation under bright illumination.

Photogate: The photogate structure, located at the edge of the photosites, provides a bias voltage for the photosites.

Transfer Gate: The transfer gate structure separates the outer edge of the photogates from the analog shift registers Charge-packets generated and accumulated in the photosites are transferred into the transport analog shift registers whenever the transfer gate voltage goes "High." All odd-numbered charge packets are transferred into the "A" transport analog shift register; all even-numbered charge packets are transferred into the "B" transport analog shift register. The transfer gate also controls the input of charge from V_{EI} into the white reference cells (described below). The time interval between successive transfer pulses determines the integration time.

Analog Shift Registers: Four 529-element analog shift registers transport charge towards the output end of the chip. The two inner registers, the transport registers, move the image-generated charge packets serially to the two gated charge detectors and amplifiers. The two outer shift registers, the peripheral registers, accumulate charge generated at the chip periphery (by photons passing through unavoidable gaps in the light shield layer, etc) and transport it to charge sinks The primary shift register clock is ϕ_T. The complementary phase relationship of the secondary shift register clocks $\overline{\phi_T}$ and $\overline{\overline{\phi_T}}$, generated on-chip, provide alternate delivery of charge packets from "A" and "B" shift registers to their amplifiers so that the original serial sequential string of video information may be easily demultiplexed off-chip.

Gated Charge Detectors & Reset Gates: Each transport analog shift register delivers charge packets to a precharged diode. The change in diode potential is linearly proportional to the amount of charge delivered in the charge packet. This potential is applied to the input gate of a MOS transistor amplifier (see below), which linearly amplifies the input potential. The diode is reset to the reset drain bias voltage (V_{RD}) by the reset gate structure. Reset occurs when both the internal reset clocks ($\overline{\overline{\phi_T}}$ on the "A" side, $\overline{\phi_T}$ on the "B" side) are "High " Each side is reset just before the next charge packet is delivered from its respective transport analog shift register.

Output Amplifiers and Sample-and-Hold Gates: Each sides' gated charge integrator drives the input of a two-stage linear MOS-transistor amplifier A schematic diagram of this circuit is shown in Figure 9 below The two stages of each amplifier are separated by sample-and-hold gates. The output of the first stage is connected to the input of the second stage whenever the sample-and-hold gate is "High." The output of the second stage is connected to the $VIDEO_{OUT}$ pin. The sample-and-hold gates are switching MOS transistors: clocking these gates results in a sampled-and-held output, thus eliminating the reset clock feedthrough. When on-chip sample-and-hold is used, pin 2 is to be tied to pin 3 and pin 21 is to be tied to pin 22. Off-chip sample-and-hold pulses can be supplied through pins 2 and 22. The sample-and-hold operation can be disabled by tying pins 2 and 22 to V_{DD}. Whenever on-chip sample-and-hold is not used, pins 3 and 21 should be left unconnected.

Clock Driver Circuits: Two MOSFET clock-driver circuits on-chip allow sample-and-hold operation of the CCD133A with only two externally-supplied clocks: the square-wave primary shift register transport clock ϕ_T, which determines the output data rate, and the transfer clock ϕ_x, which determines the integration time.

Dark and White Reference Cells and Circuitry: At each end of the 1024-photosite array there are four additional sensing elements covered by opaque metallization. These "Dark

Fig. 2 TEST LOAD CONFIGURATION

V_{DD}

DEFINITION OF TERMS

Charge-Coupled Device—A charge-coupled device is a semiconductor device in which finite isolated charge-packets are transported from one position in the semiconductor to an adjacent position by sequential clocking of an array of gates. The charge-packets are minority carriers with respect to the semiconductor substrate.

Transfer Clock ϕ_X—The transfer clock is the voltage waveform applied to the transfer gate to move the accumulated charge from the image sensor elements to the CCD transport shift registers.

Transport Clock ϕ_T—The transport clock is the clock applied to the gates of the CCD transport shift registers to move the charge-packets received from the image sensor elements to the gated charge-detector/amplifiers.

Sample-and-Hold Clock (ϕ_{SHCA}, ϕ_{SHCB}) — The voltage waveform applied to the sample-and-hold gates in the output amplifiers to create a continuous sampled video signal at the output. The sample-and-hold feature may be defeated by connecting ϕ_{SHQA} and ϕ_{SHQB} to V_{DD}.

Isolation Cell—A site on-chip producing an element in the video output that serves as a buffer between valid video data and dark reference signals. The output from an isolation cell contains no valid information and should be ignored.

Dynamic Range—The saturation exposure divided by the rms temporal noise equivalent exposure. Dynamic range is sometimes defined in terms of peak-to-peak noise. To compare the two definitions a factor of four to six is generally appropriate in that peak-to-peak noise is approximately equal to four to six times rms noise.

RMS Noise Equivalent Exposure—The exposure level that gives an output signal equal to the rms noise level at the output in the dark.

Saturation Exposure—The minimum exposure level that will provide a saturation output signal. Exposure is equal to the light intensity times the photosite integration time.

Charge Transfer Efficiency—Percentage of valid charge information that is transferred between each successive stage of the transport registers.

Responsivity—The output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure.

Total Photoresponse Non-uniformity—The difference of the response levels of the most and the least sensitive element under uniform illumination. Measurement of PRNU excludes first and last elements.

Dark Signal—The output signal in the dark caused by thermally generated electrons that is a linear function of the integration time and highly sensitive to temperature. (See accompanying photos for details of definition.)

Saturation Output Voltage—The maximum useable signal output voltage. Charge transfer efficiency decreases sharply when the saturation output voltage is exceeded.

Integration Time—The time interval between the falling edge of any two successive transfer pulses (ϕ_X). The integration time is the time allowed for the photosites to collect charge.

Pixel—A picture element (photosite).

PHOTOELEMENT DIMENSIONS

ABSOLUTE MAXIMUM RATINGS (Above which useful life may be impaired)

Storage Temperature	-25°C to +125°C
Operating Temperature (See Curves)	-25°C to +70°C
CCD133A Pins 2, 3, 4, 8, 11, 12, 14, 15, 16, 17, 18, 21, 22, 24	-0.3V to +18V
Pin 13	0V
Pins 5, 6, 7, 9, 10, 19, 20	NC
Pins 1, 23	See Caution Note

CAUTION NOTE: These devices have limited built-in gate protection. It is recommended that static discharge be controlled and minimized. Care must be taken to avoid shorting pins V_{OUT} A&B to V_{SS} or V_{DD} during operation of these devices. Shorting these pins temporarily to V_{SS} or V_{DD} may destroy the output amplifiers.

D P =

				UNITS
V_{CD}		13.5	14.5	
	Clock Driver Drain Supply Current		15	mA
		13.5		
			25	
		5.5		
V_{SS}	Substrate (Ground)			
V_{RD}		12	14.5	V

C

$V_{\phi XH}$, $V_{\phi 1}$,			11.5	

NOTES:

1. T_P is defined as the package temperature, measured on a copper block in good thermal contact with the entire backside of the package
2. ALL V_{SS} PINS MUST BE GROUNDED. All NC pins must be left unconnected.
3. V_{DD} pins may be connected to V_{CD} and/or V_{RD} pins
4. $V_T = 0.55\ \phi_{X\ HIGH} = 0.55\ \phi_{T\ HIGH}$
5. V_{EI} is used to generate the white reference output. These two signals can be eliminated by connecting V_{EI} to V_{DD}.
6. Negative transients on any clock pin going below 0.0 volts may cause charge injection, which results in an increase in apparent DS
7. C ϕ_T = 360 pF; C ϕ_X = 80 pF
   All clock rise and fall times should be > 30ns.
8. The minimum clock frequency is limited by increases in dark signal.
9. $f_{DATA} = 2\ (f\ \phi_T)$
10. OCLI WBHM = Optical Coating Laboratory, Inc. Wide Band Hot Mirror
11. CTE is the measurement for a one-stage transfer.
12. See photographs for PRNU definitions.
13. Video mismatch is the difference in ac amplitudes between $V_{OUT\ A}$ and $V_{OUT\ B}$ under uniform illumination. It can be eliminated by attenuation/amplification of one of the video outputs.
14. DC mismatch is the difference in dc output level V_O between $V_{OUT\ A}$ and $V_{OUT\ B}$.
15. See photographs for dark signal definitions.
16. Dark signal component approximately doubles for every 5-10 °C in T_P.
17. Each SPDSNU is measured from the DS level adjacent to the base of the SPDSNU. The SPDSNU approximately doubles for every 5-15 °C in T_P.
18. V_{RD} voltages in the lower range improves amplifier linearity

AC CHARACTERISTICS: (Note 1)
T_P = 25°C, f_{DATA} = 5.0 MHz, t_{int} = 1 0 ms, Light Source* = 2854°K + 2.0 mm thick Schott BG-38 and OCLI WBHM filters All tests done using "Test Load Configuration." All operating voltages nominal specified values

SYMBOL	CHARACTERISTIC	RANGE MIN	RANGE TYP	RANGE MAX	UNITS	CONDITIONS
	Dynamic Range (relative to peak-to-peak noise)		0.00009			
	(relative to rms noise)				μj/cm²	
			8.0			
			60			
		0.5		2.0		
			1.8			

OCLI WBHM = Optical Coating Laboratory, Inc Wide Band Hot Mirror

** PRNU measurements include both register outputs but exclude the outputs from the first and last elements of the array Also excluded from the measurement are video and dc mismatch

All PRNU measurements taken at 800 mV output level using an f/5.0 lens.

The "f" number is defined as the distance from the lens to the array divided by the diameter of the lens aperture. As the "f" number increases, the resulting more highly collimated light causes the package window imperfections to dominate and increase PRNU. A lower "f" number results in less collimated light causing device photosite blemishes to dominate the PRNU.

Fig. 3 TEST LOAD CONFIGURATION

MODULATION TRANSFER
FUNCTIONS FOR TWO BROADBAND
ILLUMINATION SOURCES

SPATIAL FREQUENCY — Cycles/mm

2854°K TUNGSTEN
— WITH BG-38 AND —
WBHM FILTERS

MODULATION TRANSFER
FUNCTIONS FOR NARROW BAND
ILLUMINATION SOURCES

NORMALIZED SPATIAL FREQUENCY

OUTPUT SIGNAL LEVEL
VERSUS INTEGRATION TIME
2854°K TUNGSTEN SOURCE
WITH BG-38 AND WBHM FILTERS

SIGNAL OUTPUT / SATURATION OUTPUT × 100%

t_{int} — INTEGRATION TIME — ms

SINGLE-PIXEL DARK
SIGNAL NON-UNIFORMITIES
VERSUS INTEGRATION TIME

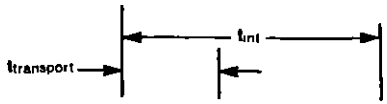
DC AND LOW-FREQUENCY
DARK SIGNAL VS INTEGRATION TIME

t_{int} — INTEGRATION TIME — ms

*RELATIVE RADIANT FLUX
VS WAVELENGTH

— — — 2854°K LIGHT SOURCE +WBHM + 2.0 mm THICK BG-38
——— 2854°K LIGHT SOURCE + 3.0 mm THICK 1-75

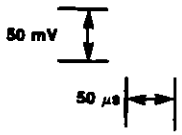
Fig. 4 PHOTORESPONSE NON-UNIFORMITY PARAMETERS (PRNU)



Zero Reference Level = 800 mV Output A Voltage

Zero Reference Level = 800 mV Output B Voltage

Peak-to-Peak Without Single-Pixel Positive and Negative Rises



TEST CONDITIONS
T_P = +25° C, f_{DATA} = 2.5 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Light source = 2854° K tungsten + 2.0 mm thick Schott BG-38 and OCLI WBHM filters. PRNU measurements taken at an output voltage of = 800 mV. Output fed through 5 MHz low pass filter.

Fig. 5 PHOTORESPONSE NON-UNIFORMITY PARAMETERS (PRNU)

Single-Pixel Negative Pulse Amplitude = 72 mV

Single-Pixel Positive Pulse Amplitude = 42 mV

TEST CONDITIONS
T_P = +25°C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Light source = 2854°K tungsten +2.0 mm thick Schott BG-38 and OCLI WBHM filters. PRNU measurements taken at an output voltage of = 800 mV. Output fed through 5 MHz low pass filter.

Fig. 6 DARK SIGNAL P

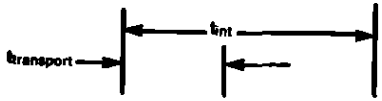
Sample-and-Hol
Clock Couplin

Average of Adjacent Pixel Outputs

Single Pixel Dark Signal Non-Uniformity (SPDNU) Amplitude = 18 mV

TEST CONDITIONS
T_P = +25°C, f_{DATA} = 5 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Output fed through 5 MHz low pass filter

Fig. 6 DARK SIGNAL PARAMETERS (DS)

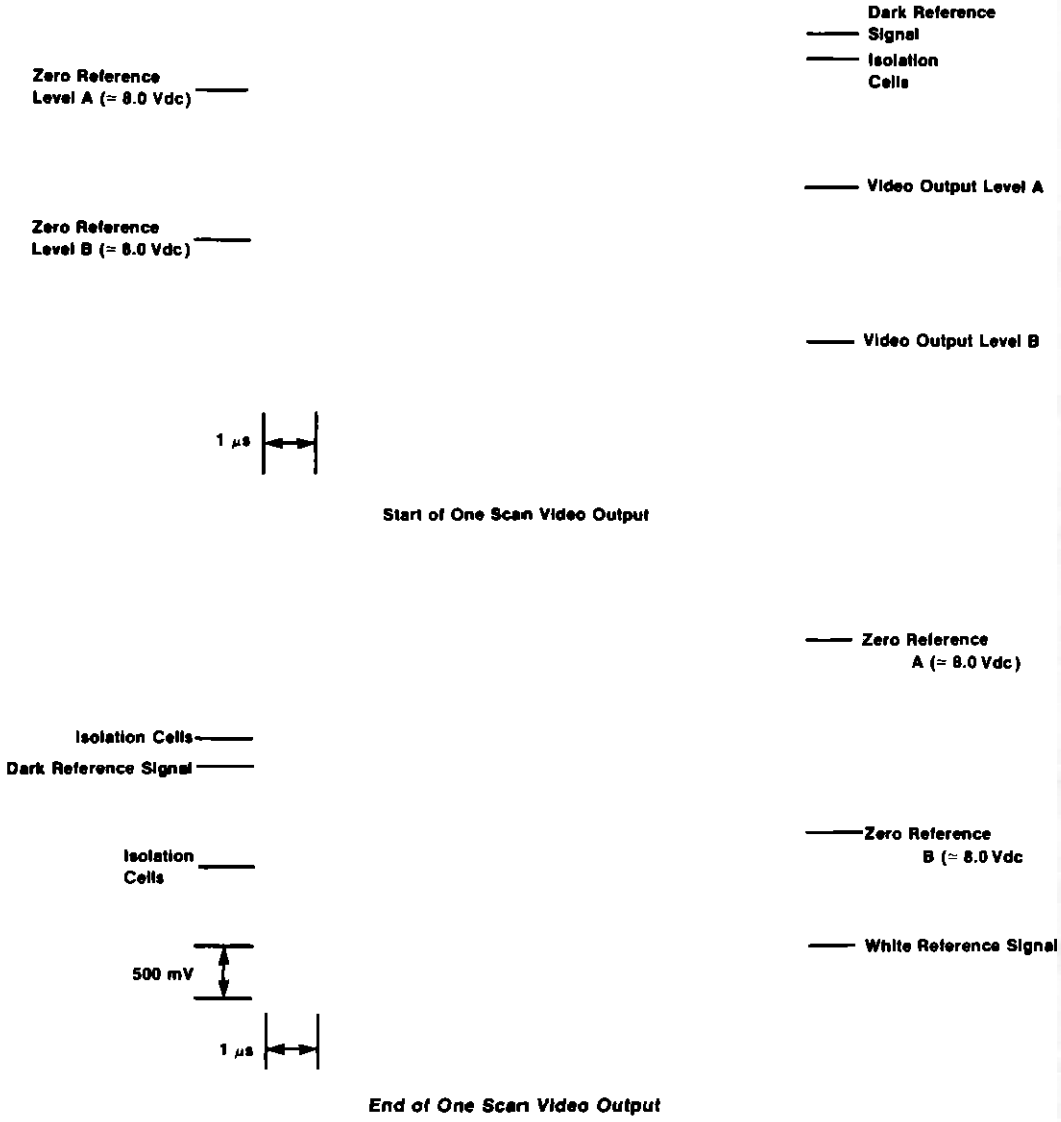


Zero Reference

5 mV

TEST CONDITIONS
T_P = +25°C, f_{DATA} = 2.5 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Output fed through 5 MHz low pass filter.

Fig. 7 VIDEO OUTPUT TIMING PHOTOGRAPHS



TEST CONDITIONS
T_P = +25°C, f_{DATA} = 5 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Light source = 2854° K tungsten with 2.0 mm thick Schott BG-38 and OCLI WBHM filters. Output fed through 5 MHz low pass filter

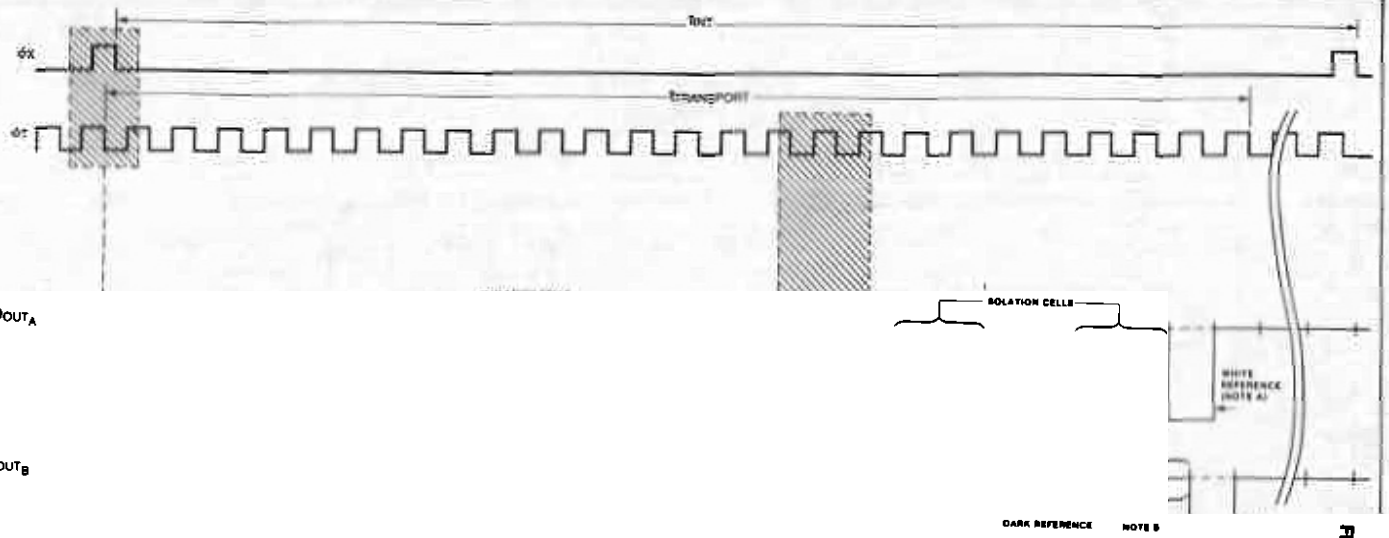


Fig. 8 TIMING DIAGRAM

DEVICE CARE AND OPERATION

Glass may be cleaned by saturating a cotton swab in alcohol and lightly wiping the surface. Rinse off the alcohol with deionized water. Allow the glass to dry, preferably by blowing with filtered dry N_2 or air.

It is important to note in design and applications considerations that the devices are very sensitive to thermal conditions. The dark signal dc and low frequency components approximately double for every 5° C temperature increase and single-pixel dark signal non-uniformities approximately double for every 8° C temperature increase. The devices may be cooled to achieve very long integration times and very low light level capability.

ORDER INFORMATION

Order CCD133ADC where "D" stands for a ceramic package and "C" for commercial temperature range.

Also available are printed circuit boards that include all the necessary clocks, logic drivers and video amplifiers to operate the CCD133A. The boards are fully assembled and tested and require only one power supply for operation (+20V). The printed circuit board order codes are CCD133DB. The CCD153A, 143A and 133A can be operated in the same printed circuit board. The 24 pin CCD133A and 153A devices are to be placed at the center of the 28 pin socket on the printed circuit board. (Note: the series resistors between the clock drivers and the CCD ϕX and ϕT pins have to be adjusted for each device type.)

NOTE: $\overline{\phi T}$ AND $\overline{\overline{\phi T}}$ ARE INTERNALLY GENERATED RESET CLOCKS.

CCD133ADC PACKAGE OUTLINE

24-Pin Dual In-line Ceramic Package

0.020 REF.
(0.508)

NOTES:
All dimensions in inches (**bold**) and millimeters (parentheses). Header is black ceramic (Al_2O_3). Window is glass. The amplifier of the device is located near the notched end of the package.

FAIRCHILD WESTON

CCD IMAGING DIVISION

CCD134
1024-Element High-Speed Linear Image Sensor

PRELIMINARY

FEATURES:

- 1024 × 1 photosite array
- 13μm × 13μm photosites on 13μm pitch
- Anti-blooming and integration control
- Enhanced spectral response (particularly in the blue region)
- Improved low-light-level performance over CCD133A
- Low dark signal
- High responsivity
- High-speed operation
- On-chip clock drivers
- Dynamic range typical: 7500:1
- Over 1V peak-to-peak outputs
- Dark and white references contained in sample-and-hold outputs
- Special selections available — consult factory.

GENERAL DESCRIPTION

PIN NAME	DESCRIPTION
V_{OUT_A}	Output Amplifier A Source

PIN CONNECTION DIAGRAM (TOP VIEW)

V_{OUT_A}	1	24	)D
ϕSHG_A	2	23	)UT$_B$
ϕSHC_A	3	22	iHGB
V_{CD}	4	21	iHCB
NC	5	20	G
NC	6	19	iAS
V_{CG}	7	18	
V_{SINK}	8	17	
		16	
		15	
		14	G
			S

Fairchild Weston Systems, Inc. CCD Imaging Division.
810 W. Maude Ave., Sunnyvale, California 94086
(408) 720-7600, TWX 910-373-2110

The CCD134 is similar to the CCD133A except for the additional features of anti-blooming and integration control. The CCD134 is a third generation device having an overall improved performance compared with first and second generation devices, including enhanced blue response and excellent low light level performance. The device incorporates on-chip clock driver circuitry and is capable of high-speed operation up to a 20MHZ data rate. The photoelement size is 13μm (0.51 mils) × 13μm (0.51 mils) on 13μm (0 51 mils) centers The device is manufactured using Fairchild Weston advanced charge-coupled device n-channel Isoplanar buried-channel technology.

FUNCTIONAL DESCRIPTION

The CCD134 consists of the following functional elements illustrated in the block diagram and circuit diagram (Fig. 1).

Photosites — A row of 1024 image sensor elements separated by a diffused channel stop and covered by a silicon dioxide surface passivation layer. Image photons pass through the transparent silicon creating hole-electron pairs. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated in each photosite is a linear function of the incident illumination intensity and the integration period. The output signal will vary in an analog manner from a thermally generated background level at zero illumination to a maximum at saturation under bright illumination.

Transfer Gates — This gate is a structure adjacent to the row of image sensor elements. The charge packets accumulated in the photosites are transferred in parallel via the transfer gate to the transport shift registers whenever the transfer gate voltage goes high. Alternate charge packets are transferred to the A and B transport registers

Four 529 Bit Analog Transport Shift Registers — Two registers are on each side of the line of image sensor elements and are separated from it by the transfer gate. The two inside registers, called the transport shift registers are used to move the light generated charge packets delivered by the transfer gates serially to the charge detector amplifier. The complementary phase relationship of the last elements of the two transport registers provides for alternate delivery of charge packets at the output amplifiers. The outer two registers serve to reduce peripheral electron noise in the inner shift registers.

Two Gated Charge Detector/Amplifiers — Charge packets are transported to a precharged capacitor whose potential changes linearly in response to the quantity of the signal charge delivered This potential is applied to the input gate of the two-stage NMOS amplifiers producing a signal at the output "V_{OUT}" pins. The sample-and-hold gate is a switching MOS transistor in the output amplifier that allows the output to be delivered as a sample-and held waveform. The diode is recharged internally before the arrival of each new signal charge-packet from the transport shift register.

Integration and Anti-Blooming Control — In many applications the dynamic range in parts of the image is larger than the dynamic range of the CCD, which may cause more electrons to be generated in the photosite area than can be stored in the CCD shift register. This is particularly common in Industrial inspection and satellite applications. The excess electrons generated by bright illumination tend to "bloom" or "spill over" to neighboring pixels along the shift register, thus "smearing" the information. This smearing can be eliminated using two methods:

Anti-Blooming Operation:

A DC voltage applied to the integration control gate (approximately 5 to 7 volts) will cause excess charge generated in the photosites to be diverted to the anti-blooming sink (V_{SINK}) instead of to the shift registers. This acts as a "clipping circuit" for the CCD output (see Fig. 2). (See also page 238 for further details)

Integration Control Operation:

Variable integration times which are less than the CCD exposure time may be attained by supplying a clock to the integration control gate. Clocking ϕ_{IC} reduces the photosite signal in all photosites by the ratio $t_{EXPOSURE}/t_{INT}$. Greater than 10:1 reduction in the average photosite signal can be achieved with integration control.

The integration-control and anti-blooming features can be implemented simultaneously. This is done by setting the ϕ_{IC} clock-low level to approximately 5 to 7 volts. (See application note on page 238 for further discussion).

Fig. 1 BLOCK DIAGRAM

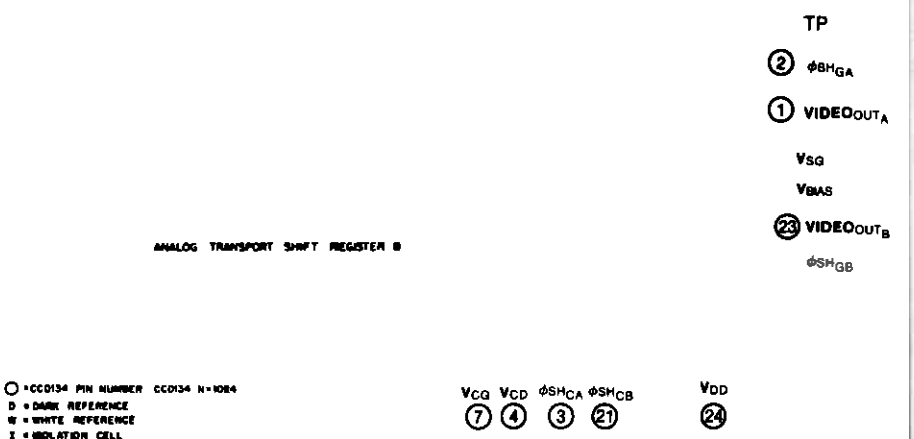


Fig. 2 MAXIMUM OUTPUT VOLTAGE vs. ϕ_{IC} VOLTAGE

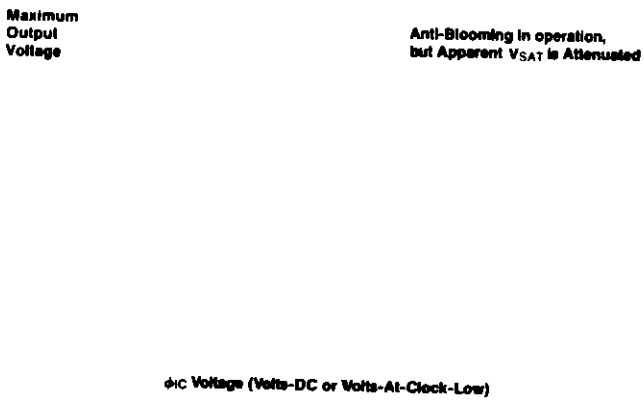


Fig. 3 INTEGRATION-CONTROL TIMING DIAGRAM AND NOTES

NOTES:

1 t_I > t_{fall} of ϕ_X.

nto the shift registers during ϕ_X clock-high period. Photosite charge > Q_{SAT} mized.
(see Fig. 2).
IC into V_{OUT}.
7 volts.
ts DC or V_{SS}.

voltage.

Fig. 5 TEST LOAD CONFIGURATION (INTERNAL SAMPLE-AND-HOLD DISABLED)

DEFINITION OF TERMS

Charge-Coupled Device — A charge-coupled device is a semiconductor device in which finite isolated charge packets are transported from one position in the semiconductor to an adjacent position by sequential clocking of an array of gates. The charge packets are minority carriers with respect to the semiconductor substrate.

Sample-and-Hold Clock (ϕSHCA, ϕSHCB) — The voltage waveform for triggering the sample-and-hold gates in the output amplifiers to create a continuous sampled video signal at the output. The sample-and-hold feature may be defeated by connecting ϕSHGA and ϕSHGB to V_{DD}. Use of the internal sample-and-hold capability is possible for data rates up to 13MHz. For use above 13MHz consult factory.

Dark Reference — Video output level generated from sensing elements covered with opaque metalization which provides a reference voltage equivalent to device operation in the dark. This permits use of external DC restoration circuitry.

Isolation Cell — This is a site on-chip producing an element in the video output that serves as a buffer between valid video data and dark reference signals The output from an isolation cell contains no valid information and should be ignored.

Dynamic Range — The saturation exposure divided by the RMS temporal noise equivalent exposure. Dynamic range is sometimes defined in terms of peak-to-peak noise. To compare the two definitions a factor of four to six is generally appropriate in that peak-to-peak noise is approximately equal to four to six times RMS noise.

RMS Noise Equivalent Exposure — The exposure level that gives an output signal equal to the RMS noise level at the output in the dark.

Saturation Exposure — The minimum exposure level that will provide a saturation output signal. Exposure is equal to the light intensity times the photosite integration time.

Charge Transfer Efficiency — Percentage of valid charge information that is transferred between each successive stage of the transport registers.

Responsivity — The output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure.

Total Photoresponse Non-Uniformity — The difference of the response levels of the most and the least sensitive element under uniform illumination. Measurement of PRNU excludes first and last elements.

Dark Signal — The output signal in the dark caused by thermally generated electrons that is a linear function of the integration time and is highly sensitive to temperature.

Saturation Output Voltage — The maximum useable signal output voltage Charge transfer efficiency decreases sharply when the saturation output voltage is exceeded.

Integration Time — The time interval between the falling edge of the integration control clock and the falling edge of the transfer clock. The integration time is the time in which charge is accumulated in the photosites.

Exposure Time — The time interval between the falling edge of the two transfer pulses (ϕX) as shown in the timing diagram. The exposure time is the time between transfers of signal charge from the photosites into the transport registers

Pixel — A picture element (photosite).

PHOTOELEMENT DIMENSIONS

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	-25°C to +125°C
Operating Temperature	-25°C to +70°C
CCD 134: Pins 2, 3, 4, 7, 8, 9, 10, 11, 12, 14, 15, 16, 17, 19, 21, 22, 24	-0.3V to 18V
Pin 20	0.0V to +0.7V
Pin 13	-3.0V to 0V
Pins 5, 6, 18	NC
Pins 1, 23	SEE CAUTION NOTE

CAUTION NOTE:
These devices have limited built-in gate protection. It is recommended that static discharge be controlled and minimized. Care must be taken to avoid shorting pins $VIDEO_{OUT_{A+B}}$ to V_{SS}, V_{SG}, V_{CG} or V_{DD} during operation of the devices. Shorting these pins temporarily to V_{SS}, V_{SG}, V_{CG} or V_{DD} may destroy the output amplifiers.

DC CHARACTERISTICS: T_P = 25°C (Note 1, 2) Use typical values for optimum performance

	CHARACTERISTIC					
V_{CD}	Clock Driver Drain Supply Voltages	13.5	14.0	14.5	V	
V_{DD}	Output Amplifier Drain Supply Voltage	13.5	14.0	14.5	V	
V_{SINK}	Anti-Blooming Sink Voltage	13.5	14.0	14.5	V	
V_{BIAS}	Amplifier Bias Voltage	3.0	3.5	4.0	V	
V_{PG}	Photogate Bias Voltage	5.5	6.0	6.5	V	
V_T	Shift Register DC Electrode Bias Voltages	5.5	6.0	6.5	V	Note 3
V_{EI}	Electrical Input Bias Voltage		10.5		V	Note 4
V_{CG}	Clock Ground	0.0	0.3	0.7	V	
V_{SG}	Amplifier Signal Ground	0.0	0.3	0.7	V	
V_{SS}	Substrate Ground	-3.0	-2.0	-1.0	V	Note 5
I_{CD}	Clock Driver Supply Current	0.0	7.0	15.0	mA	
I_{DD}	Output Amplifier Drain Supply Current		15.0	25.0	mA	

CLOCK CHARACTERISTICS: T_P = 25°C (Note 1) Use typical values for optimum performance

$V_{\phi X\ HIGH}$			11.5	V	Note 6
$V_{\phi T\ HIGH}$			11.5	V	Note 6
$V_{\phi IC\ HIGH}$		GH	11.5	V	Note 6
$V_{\phi X\ LOW}$			0.3	V	Notes 5, 6
$V_{\phi T\ LOW}$			0.3	V	Notes 5, 6
$V_{\phi IC\ LOW}$		)W	6.0	V	Note 15
f_{data} max			20.0	MHz	Notes 7, 8

AC CHARACTERTISTICS: $T_P = 25°C$ (Note 1), $f_{data} = 5.0MHz$, $t_{int} = 1.0$ ms, Light Source = 2854° K + 2.0mm thick Schott BG-38 and OCLI WBHM Filters (Note 9), internal sample-and-hold enabled. All tests done using "Test Load Configuration

		1500:1
		7500:1
		44×10^{-6}
		0.33
.99995		.99999
		6.0
		0.75

	TYP	MAX	
Photoresponse Non-uniformity			
Peak-to-Peak	60	160	mV
Peak-to-Peak without single pixel and Positive and Negative Pulses	40		mV
Single-pixel Positive Pulses			mV
Single-pixel Negative Pulses			mV
Video Mismatch			mV
DC Mismatch			V
Dark Signal:			
DC Component	1		mV
Low Frequency Component	1		mV
Single Pixel DS Non-Uniformity	1		mV
Responsivity	4.5		V/μJ/cm²
Saturation Output Voltage	1.5		V

NOTES:

* All PRNU measurements taken at an 800 mvolt output level

resulting more highly collimated light causes the package window imperfections less collimated light causing device photosite blemishes to dominate the PRNU.

NOTES:

1. T_P is defined as the package temperature measured on a copper block in good thermal contact with the entire backside of the package.
2. NC pins must be left unconnected
3. V_T = 0.55 ϕX_{HIGH} = 0.55 ϕT_{HIGH}
4. V_{EI} is used to generate the white reference outputs. *These two signals can be reduced by connecting V_{EI} to V_{DD}.*
5. Negative transients on any clock pin going below 0.0 volts may cause charge injection, which results in an increase in apparent DS. Adjusting V_{SS} to a more negative voltage than the clock low voltages will reduce charge injection, if present.
6. Pin Capacitances:
   C ϕT = 300 pF; C ϕX = 80 pF.
7. The minimum clock frequency is limited by increases in dark signal
8. $f_{data} = 2 (f \phi T)$
9. OCLI WBHM = Optical Coating Laboratory, Inc. Wide Band Hot Mirror.

11. Video mismatch is the difference in AC amplitudes between V_{OUT_A} and V_{OUT_B} under uniform illumination. It can be eliminated by attenuation/amplification of one of the video outputs.
12. DC mismatch is the difference in DC output level V_O between V_{OUT_A} and V_{OUT_B}.
13. Dark signal component approximately doubles for every 5-10 °C in T_P.
14. Each SPDSNU is measured from the DS level adjacent to the base of the SPDSNU. The SPDSNU approximately doubles for every 5-15 °C increase in T_P.
15. See definitions of Anti-Blooming Control and Integration Control

TYPICAL PERFORMANCE CURVES

MODULATION TRANSFER FUNCTIONS FOR TWO BROADBAND ILLUMINATION SOURCES

MTF — MODULATION TRANSFER FUNCTION

MODULATION TRANSFER FUNCTIONS FOR NARROW BAND ILLUMINATION SOURCES

SPATIAL FREQUENCY — Cycles/mm

TYPICAL SPECTRAL RESPONSE

RELATIVE IRRADIANCE (%)

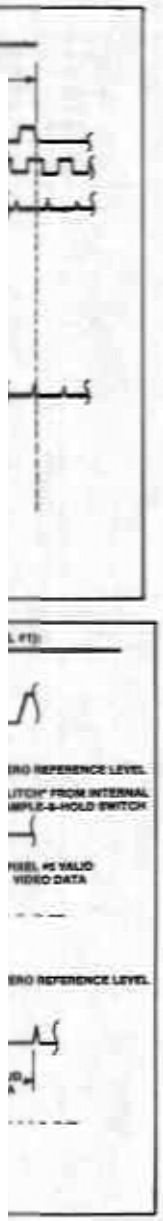
WAVELENGTH (nm)

——— TYPICAL "DAYLIGHT FLUORESCENT" BULB
— — — 2854° K LIGHT SOURCE +WBHM + 2 0 mm THICK BG-38
——— 2854° K LIGHT SOURCE + 3 0 mm THICK 1-75

DC AND LOW-FREQUENCY DARK SIGNAL VS INTEGRATION TIME

DC & LOW-FREQUENCY DARK SIGNAL — mV

TIMING DIAGRAM (Internal Sample & Hold Enabled, See Fig. 5)

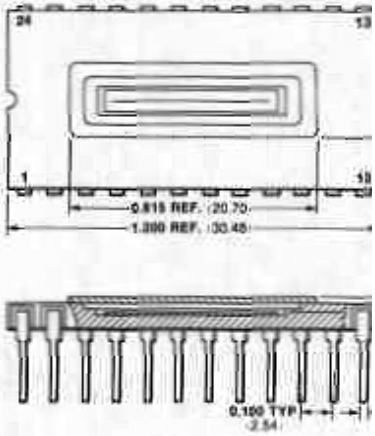


$t_{\phi X_{CH}}$ > 60 ns MINIMUM; 500-1000 ns PREFERRED
$t_{\phi T_{CH}}$ > 50 ns. 50% DUTY CYCLE PREFERRED.
t_1, t_3 > 10 ns
t_2 > 30 ns
t_{RISE}, t_{FALL} ≥ 10 ns MINIMUM (> 20 ns PREFERRED)
FOR BOTH ϕ_X AND ϕ_T

GENERAL NOTES

1. White reference cell output signals will be approximately equal in height. This output can be reduced by connecting V_{EI} to V_{DD}.
2. The isolation cells may contain output signals as part of their buffer function. These signals should be disregarded.
3. Integration control clock (ϕ_{IC}) omitted for clarity. Refer to "Integration control clock timing diagram" (Figure 3) for details

PAC
24-Pin Dual



NOTES:
All dimensions in inches (bold) and millimeters (parentheses). Header is black ceramic (Al_2O_3). Window is glass. The amplifier of the device is located near the notched end of the package.

FAIRCHILD WESTON

CCD IMAGING DIVISION

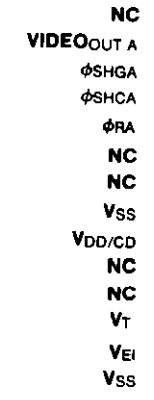
CCD143A
2048-Element High-Speed Linear Image Sensor

FEATURES

- 2048 × 1 photosite array
- 13μm × 13μm photosites on 13μm pitch
- High Speed: up to 20 MHz data rate
- Enhanced spectral response
- Low dark signal
- High responsivity
- On-chip clock drivers
- Dynamic range typical: 7500:1
- Over 1 V peak-to-peak outputs
- Optional facility for correlated double sampling
- Dark and white references contained in sample-and-hold outputs
- Special selections available — consult factory

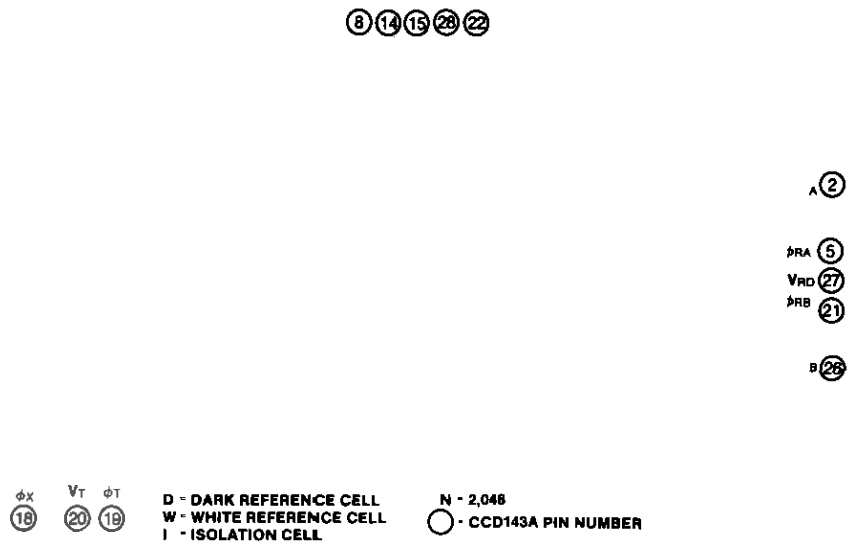
PIN NAMES	DESCRIPTION
V_{PG}	Photogate
V_{CG}	Sample-and-Hold Clock Ground
V_{RD}	Reset Transistor Drain
V_{EI}	Electrical Input Bias
V_T	Analog Transport Shift Register DC Electrode
ϕSHGA	Sample-and-Hold Gate A
ϕSHCA	Sample-and-Hold Clock A
ϕSHGB	Sample-and-Hold Gate B
ϕSHCB	Sample-and-Hold Clock B
ϕRA	Reset Clock A
ϕRB	Reset Clock B
VSS	Substrate (GND)
NC	No Connection (Do not ground)

PIN CONNECTION DIAGRAM (TOP VIEW)



Fairchild Weston Systems, Inc. CCD Imaging Division
810 W. Maude Ave., Sunnyvale, California 94086
(408) 720-7600, TWX 910-373-2110

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The CCD143A consists of the following functional elements illustrated in the Block Diagram:

Image Sensor Elements — These are elements of a line of 2048 image sensors separated by diffused channel stops and covered by a silicon dioxide surface passivaton layer Image photons pass through the transparent silicon dioxide layer and are absorbed in the single crystal silicon creating hole-electron pairs. The photon generated electrons are *accumulated in the photosites The amount of charge* accumulated in each photosite is a linear function of the incident illumination intensity and the integration period The output signal will vary in an analog manner from a thermally generated noise background at zero illumination to a maximum at saturation under bright illumination.

Transfer Gate — This gate is a structure adjacent to the line of image sensor elements. The charge-packets accumulated in the image sensor elements are transferred out via the transfer gate to the transport registers whenever the transfer gate goes HIGH. Alternate charge-packets are transferred to the analog transport shift registers. The transfer gate also controls the exposure time for the sensing elements.

Four 1041-Bit Analog Shift Registers — Two registers are on each side of the line of image sensor elements and separated from it by the transfer gate. The two inside registers, called the transport shift registers, are used to move the image generated charge-packets delivered by the transfer gate serially to the two charge-detector/amplifiers. The complementary phase relationship of the last elements of the two transport shift registers provides for alternate delivery of charge-packets to the amplifiers so that the original serial sequence of the line of video may be reestablished at the outputs. The outer two registers serve to reduce peripheral electron noise in the inner shift registers.

Two Gated Charge-Detector/Amplifiers — From the end of each transport shift register, charge-packets are delivered to a precharged diode whose potential changes linearly in response to the quantity of the signal charge delivered. This potential is applied to the gate of an n-channnel MOS transistor producing a signal which passes through the sample-and-hold gate to the output at $VIDEO_{OUT}$. The sample-and-hold gate is a switching MOS transistor in the output amplifier that allows the output to be delivered as a sample-and-hold waveform. The diode is recharged internally before the arrival of each new signal charge-packet from the transport shift register.

Clock Driver Circuitry — This circuitry allows operation of the CCD143A using only two external clocks, (1) a square wave Transport Clock which controls the readout rate of video data from the sensor, and (2) a Transfer Clock pulse which controls the integration time of the sensor.

Dark and Optional White Reference Circuitry — Four additional sensing elements at both ends of the 2048 array are covered by opaque metalization. They provide a dark (no illumination) signal reference which is delivered at both ends of the line of video output representing the 2048 illuminated sensor elements (labeled "D" in the Block Diagram) Also included at one end of the 2048 sense element array is a white signal reference level generator which likewise provides a reference in the output signal (labeled "W" in the Block Diagram) These reference levels are useful as inputs to external dc restoration and/or automatic gain control circuitry. The white reference signal can be enabled by connecting V_{EI} to a DC voltage less than V_{DD} A V_{EI} voltage of 6V will typically produce a white reference signal of 80±20% of the saturation output voltage.

DEFINITION OF TERMS:

Charge-Coupled Device — A charge-coupled device is a semiconductor device in which finite isolated charge-packets are transported from one position in the semiconductor to an adjacent position by sequential clocking

of an array of gates. The charge-packets are minority carriers with respect to the semiconductor substrate.

peak-to-peak noise level at the output in the dark.

Saturation Exposure — Saturation exposure is the minimum exposure level that will produce a saturated output signal. Exposure is equal to the light intensity times the photosite integration time.

Charge Transfer Efficiency — This is the percentage of valid charge information that is transferred between each successive stage of the transport registers.

Spectral Response Range — This is the spectral band in which the response per unit of radiant power is more than 10% of the peak response.

Responsivity — Responsivity is the output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure level.

Dark Signal — This is the output signal in the dark caused by thermally generated electrons which is a linear function of integration time and highly sensitive to temperature. (See accompanying photos for details of definition.)

Total Photoresponse Non-Uniformity — This is the difference in the response levels between the most and least sensitive elements under uniform illumination. (See accompanying photos for details of definition.)

Integration Time — The time interval between the falling edges of any two successive transfer pulses ϕX is the integration time shown in the Timing Diagram. The integration time is the time allowed for the photosites to collect charge.

Pixel — Picture element (photosite).

TEST LOAD

PHOTOELEMENT DIMENSIONS

All dimensions are typical values

ABSOLUTE MAXIMUM RATINGS (Above which useful life may be impaired)

Storage Temperature	−25°C to +125°C
Operating Temperature (See curves)	−25°C to +70°C
CCD143A Pins 3, 4, 5, 9, 12, 13, 17, 18, 19, 20, 21, 24, 25, 27, 22.	−0.3V to 18V
Pins14, 15, 16, 28, 8.	0V
Pins 1, 6, 7, 11, 23	NC
Pins 2, 26.	See Caution Note

CAUTION NOTE: These devices have limited built-in gate protection. It is recommended that static discharge be controlled and minimized. Care must be taken to avoid shorting pins $VIDEO_{OUT}$ A&B to V_{SS} or V_{DD} during operation of the devices. Shorting these pins temporarily to V_{SS} or V_{DD} may destroy the output amplifiers.

V_{SS} Substrate (Ground)

Reset Transistor Drain

$V\phi_{XH}$, $V\phi_{TH}$

$f_{DATA\ MAX}$

1. T_P is defined as the package temperature, measured on a copper block in good thermal contact with the backside of the device.
2. All V_{SS} pins must be grounded. All V_{DD} pins must be connected and tied to V_{CD}. All NC pins must be left unconnected.
3. $V_{DD} = V_{CD}$.
4. $V_T = 0.55\ V\phi_{XH} = 0.55\ V\phi_{TH}$.
5. White reference signal can be enabled by connecting V_{EI} to a voltage less than V_{DD}. $V_{EI} = 6V$ will typically produce a white reference signal of 80±20% of the saturation output voltage.
6. Negative transients on any clock pin going below 0.0V may cause charge-injection which results in an increase in apparent DS. (See "Charge Injection")
7. $C_{\phi T} = 700$ pF for CCD143A, $C_{\phi X} = 300$ pF for CCD143A.
8. Minimum clock frequency is limited by increase in dark signal.
9. $f_{DATA} = 2 \times f_{\phi T}$.
10. Dynamic range is defined as V_{SAT}/peak-to-peak temporal noise or V_{SAT}/rms temporal noise.
11. 1 μJ/cm² = 0.02 f_{CS} at 2854°K, 1 f_{CS} = 50 μJ/cm² at 2854°K.
12. SE for 2854°K broadband light without 2.0 mm Schott BG-38 and OCLI WBHM filters is typically 0.8 μJ/cm².
13. CTE is the measurement for a one-stage transfer.
14. See photographs for PRNU definitions.
15. Video mismatch is the difference in ac amplitudes between $VIDEO_{OUTA}$ and $VIDEO_{OUTB}$ under uniform illumination. It can be eliminated by attenuation/amplification of one of the video outputs.
16. DC mismatch is the difference in dc output level (V_O) between $VIDEO_{OUTA}$ and $VIDEO_{OUTB}$.
17. See photographs for DS definitions.
18. Dark signal component approximately doubles for every 5°C increase in T_P.
19. Each SPDSNU is measured from the DS level adjacent to the base of the SPDSNU. The SPDSNU approximately doubles for every 6°C increase in T_P.
20. Responsivity for 2854°K broadband light source without 2.0 mm Schott BG-38 and OCLI WBHM filters is typically 2 V per μJ/cm².
21. See test load configurations.
22. Internal reset of the gated charge detector is achieved by connecting ϕ_{RA} and ϕ_{RB} to V_{DD}

AC CHARACTERISTICS: (Note 1)
T_P = 25° C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms, Light Source* = 2854° K + 2.0 mm thick Schott BG-38 and OCLI WBHM filters
All operating voltages nominal specified values. All tests done using "Test Load Configuration."

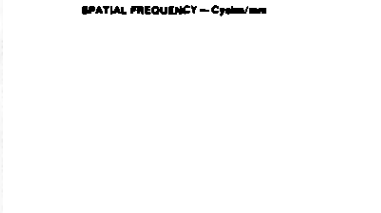
SYMBOL	CHARACTERISTIC	RANGE MIN	RANGE TYP	RANGE MAX	UNITS	CONDITIONS
DR	Dynamic Range (relative to peak-to-peak noise)		1500:1			Note 10
	(relative to rms noise)		7500:1			
			0.00009			
			0.67		μj/cm2	
			1.0			
			3.0			

All PRNU measurements are taken at a 800 mV output level using an f/5.0 lens

The "f" number is defined as the distance from the lens to the array divided by the diameter of the lens aperture. As the "f" number increases, the resulting more highly collimated light causes the package window imperfections to dominate and increase PRNU. A lower "f" number results in less collimated light causing device photosite blemishes to dominate the PRNU

TYPICAL PERFORMANCE CURVES

MODULATION TRANSFER FUNCTIONS FOR TWO BROADBAND ILLUMINATION SOURCES



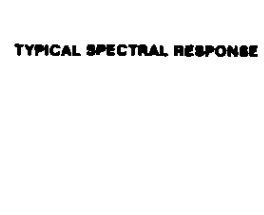
MODULATION TRANSFER FUNCTIONS FOR NARROW BAND ILLUMINATION SOURCES

OUTPUT SIGNAL LEVEL VERSUS INTEGRATION TIME 2854°K TUNGSTEN SOURCE WITH BG-38 AND WBHM FILTERS

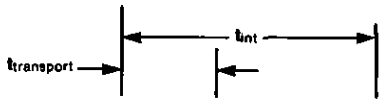
SINGLE-PIXEL DARK SIGNAL NON-UNIFORMITIES VERSUS INTEGRATION TIME

***RELATIVE RADIANT FLUX VS WAVELENGTH**

TYPICAL SPECTRAL RESPONSE



PHOTORESPONSE NON-UNIFORMITY PARAMETERS (PRNU)



Zero Reference Level ≈ 800 mV Output A Voltage

Zero Reference Level ≈ 800 mV Output B Voltage

50

Peak-to-Pe
PR

Peak-to-Peak Without Single-Pixel Positive and Negative Rises

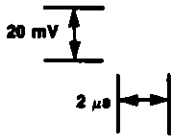
50 m

TEST CONDITIONS
T_P = +25° C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Light source = 2854° K tungsten + 2.0 mm thick Schott BG-38 and OCLI WBHM filters. PRNU measurements taken at an output voltage of ≈ 800 mV. Output fed through 5 MHz low pass filter.

PHOTORESPONSE NON-UNIFORMITY PARAMETERS (PRNU)

Single-Pixel Negative Pulse Amplitude = 72 mV

Single-Pixel Positive Pulse Amplitude = 42 mV



TEST CONDITIONS
T_P = +25°C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Light source = 2854°K tungsten +2.0 mm thick Schott BG-38 and OCLI WBHM filters. PRNU measurements taken at an output voltage of = 800 mV. Output fed through 5 MHz low pass filter.

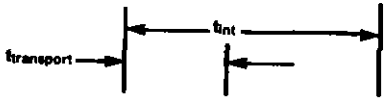
Sample-and-Ho
Clock Couplin

Average of Adjacent Pixel Outputs

Single Pixel Dark Signal Non-Uniformity (SPDNU) Amplitude = 18 mV

TEST CONDITIONS
T_P = +25°C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Output fed through 5 MHz low pass filter.

DARK SIGNAL PARAMETERS (DS)



5 r

Zero Reference

5 m

TEST CONDITIONS

T_P = +25° C, f_{DATA} = 5.0 MHz, t_{int} = 1 0 ms All voltages nominal specified values. Output fed through 5 MHz low pass filter.

VIDEO OUTPUT TIMING PHOTOGRAPHS

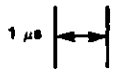
Dark Reference
Signal
Isolation
Cells

Zero Reference
Level A (≈ 8.0 Vdc)

Video Output Level A

Zero Reference
Level B (≈ 8.0 Vdc)

Video Output Level B



Start of One Scan Video Output

TEST CONDITIONS
T_P = +25° C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Light source = 2854° K tungsten = 2.0 mm thick Schott BG-38 and OCLI WBHM filters. Output fed through 5 MHz low pass filter

OUTPUT AMPLIFIER SCHEMATIC

CHARGE
PACKETS
FROM
SHIFT REG
"A"

CHARGE
PACKETS
FROM
SHIFT REG.
"B"

NOTE: $\bar{\phi}_T$ AND $\overline{\bar{\phi}_T}$ ARE INTERNALLY GENERATED RESET CLOCKS.

TIMING DIAGRAM (ϕ_{SH} ENABLED)

DEVICE CARE AND OPERATION:

Glass may be cleaned by saturating a cotton swab in alcohol and lightly wiping the surface. Rinse off the alcohol with de-ionized water. Allow the glass to dry, preferably by blowing with filtered dry N_2 or air.

It is important to note in design and applications considerations that the devices are very sensitive to thermal conditions. The dark signal dc and low frequency components approximately double for every 5° C temperature increase and single-pixel dark signal non-uniformities approximately double for every 8° C temperature increase. The devices may be cooled to achieve very long integration times and very low light level capability.

ORDER INFORMATION:

Order CCD143ADC where "D" stands for a ceramic package and "C" for commercial temperature range.

Also available are printed circuit boards that include all the necessary clocks, logic drivers, and video amplifiers to operate the CCD143ADC. The boards are fully assembled and tested and require only one power supply for operation (+20V). The printed circuit board order code is CCD143DB. The CCD133A, 143A and 153A can be operated in the same printed circuit board. The 24 pin CCD133A and CCD153A devices are to be placed at the center of the 28 pin socket on the printed circuit board.

CCD143ADC PACKAGE OUTLINE
28-Pin Dual In-line Ceramic Package

NOTES:
All dimensions in inches (bold) and millimeters (parentheses). Header is black ceramic (Al_2O_3). Window is glass. The amplifier of the device is located near the notched end of the package.

FAIRCHILD WESTON

CCD IMAGING DIVISION

CCD145 PRELIMINARY
2048-Element Linear Image Sensor

FEATURES

- 2048 × 1 photosite array
- 13μm × 13μm photosites on 13μm pitch
- Anti-blooming and integration control
- Enhanced Spectral Response (particularly in the blue region)
- Low dark signal
- Excellent low-light-level performance
- High responsivity
- Dynamic range typical: 7500:1
- Over 1V peak-to-peak outputs
- Dark reference contained in a sample-and-hold output
- Special selections available — consult factory.

DESCRIPTION

or in environments where lighting conditions are difficult.

The photoelement size is 13μm (0.51 mils) by 13μm (0.51 mils) on 13μm (0.51 mils) centers. The device is manufactured using Fairchild Weston advanced charge-coupled device n-channel Isoplanar buried-channel technology.

PIN NAMES	DESCRIPTION
V_{PG}	
ϕXA, ϕXB	
$\phi 1A$, $\phi 2A$	
$\phi 1B$, $\phi 2B$	
ϕR	
ϕSH	
$\phi ICA\phi ICB$	
$VIDEO_{OUT}$	
$COMP_{OUT}$	
V_{DD}	
V_{CD}	
RD	
OG	
V_{SINK}	
V_{BIAS}	
V_{SG}	
V_{SS}	
NC	

PIN CONNECTION DIAGRAM
(TOP VIEW)

)UT

UT

Fairchild Weston Systems, Inc. CCD Imaging Division
810 W. Maude Ave., Sunnyvale, California 94086
(408) 720-7800, TWX 910-373-2110

FUNCTIONAL DESCRIPTION

The CCD145 consists of the following functional elements illustrated in the Block Diagram:

Image Sensor Elements — A row of 2048 image sensor elements separated by a diffused channel stop and covered by a silicon dioxide surface passivation layer. Image photons pass through the transparent silicon dioxide layer and are absorbed in the single crystal silicon, creating hole-electron pairs. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated in each photosite is a linear function of the incident illumination intensity and the integration period The output signal will vary in an analog manner from a thermally generated background level at zero illumination to a maximum at saturation under bright illumination.

Two Transfer Gates — Gate structures adjacent to the row of image sensor elements. The charge packets accumulated in the image sensor elements are transferred out via the transfer gates to the transport registers whenever the transfer gate voltages go HIGH. Alternate charge packets are transferred to the A and B transport registers.

Integration and Anti-Blooming Control — In many applications the dynamic range in parts of the image is larger than the dynamic range of the CCD, which may cause more electrons to be generated in the photosite area than can be stored in the CCD shift register. This is particularly common in industrial inspection and satellite applications. The excess electrons generated by bright illumination tend to "bloom" or "spill over" to neighboring pixels along the shift register, thus "smearing" the information. This smearing can be eliminated by using two methods:

Anti-Blooming Operation:

A DC voltage applied to the integration control gate (approximately 5 to 7 volts) will cause excess charge generated in the photosites to be diverted to the anti-blooming sink (V_{SINK}) instead of to the shift registers This acts as a "clipping circuit" for the CCD output (see Fig. 2). (See also page 238 for further details)

Integration Control Operation:

Variable integration times which are less than the CCD exposure time may be attained by supplying a clock to the integration control gate. Clocking ϕ_{IC} reduces the photosite signal in all photosites by the ratio $t_{EXPOSURE}/t_{INT}$. Greater than 10:1 reduction in the average photosite signal can be achieved with integration control

The integration-control and anti-blooming features can be implemented simultaneously. This is done by setting the ϕ_{IC} clock-low level to approximately 5 to 7 volts. (See application note on page 238 for further discussion).

Two Analog Transport Shift Registers — One on each side of the line of image sensor elements and are separated from it by a transfer gate. The two registers, called the transport registers, are used to move the light generated charge packets delivered by the transfer gates serially to the charge detector/amplifier. The complementary phase relationship of the last elements of the two transport registers provides for alternate delivery of charge packets to establish the original serial sequence of the line of video in the output circuit.

A Gated Charge Detector/Amplifier — Charge packets are transported to a precharged diode whose potential changes linearly in response to the quantity of the signal charge delivered. This potential is applied to the gate of an n-channel MOS transistor producing a signal at the output $VIDEO_{OUT}$. A reset transistor is driven by the reset clock (ϕ_R) and recharges the charge detector diode before the arrival of each new signal charge packet from the transport registers.

DEFINITION OF TERMS

Charge-Coupled Device — A charge-coupled device is a semiconductor device in which finite isolated charge packets are transported from one position in the semiconductor to an adjacent position by sequential clocking of an array of gates. The charge packets are minority carriers with respect to the semiconductor substrate.

Transfer Clocks ϕ_{XA}, ϕ_{XB} — The voltage waveforms applied to the transfer gates to move the accumulated charge from the image sensor elements to the CCD transport registers.

Transport Clocks ϕ_{1A}, ϕ_{2A}, ϕ_{1B}, ϕ_{2B} — The two sets of 2-phase waveforms applied to the gates of the transport registers to move the charge packets received from the image sensor elements to the gated charge detector/amplifier.

Sample-and-Hold Clock ϕ_{SH} — The voltage waveform applied to the sample-and-hold gate in the output amplifier to create a continuous sampled video signal at the output. The sample-and-hold feature may be defeated by connecting ϕ_{SH} to V_{DD}.

Reset Clock ϕ_R — The voltage waveform required to reset the voltage on the charge detector.

Dark Reference — Video output level generated from sensing elements covered with opaque metalization which provides a reference voltage equivalent to device operation in the dark. This permits use of external DC restoration circuitry.

Isolation Cell — This is a site on-chip producing an element in the video output that serves as a buffer between valid video data and dark reference signals. The output from an isolation cell contains no valid video information and should be ignored.

Dynamic Range — The saturation exposure divided by the rms noise equivalent exposure. Dynamic range is sometimes defined in terms of peak-to-peak noise. Peak-to-peak noise is generally equal to four to six times rms noise.

RMS Noise Equivalent Exposure — The exposure level that gives an output signal equal to the rms noise level of the output in the dark.

Saturation Exposure — The minimum exposure level that will provide a saturation output signal. Exposure is equal to the light intensity times the photosite integration time.

Charge Transfer Efficiency — Percentage of valid charge information that is transferred between each successive stage of the transport registers.

Responsivity — The output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure.

Total Photoresponse Non-uniformity — The difference of the response levels of the most and the least sensitive element under uniform illumination. Measurement of PRNU excludes first and last elements.

Dark Signal — The output signal in the dark caused by thermally generated electrons. It is a linear function of the integration time and is highly sensitive to temperature.

Saturation Output Voltage — The maximum useable signal output voltage. Charge transfer efficiency decreases sharply when the saturation output voltage is exceeded.

Exposure Time — The time interval between the falling edges of any two transfer pulses ϕ_{XA} or ϕ_{XB} as shown in the timing diagram. The exposure time is the time between transfers of signal charge from the photosites into the transport registers.

Pixel — A picture element (photosite).

Integration Time — The time elapsed from the falling edge of the integration control clock to the falling edge of the transfer clock. The integration time is the time in which charge is accumulated in the photosites.

TEST LOAD CONFIGURATION

VIDEO$_{OUT}$

COMP$_{OUT}$

ABSOLUTE MAXIMUM RATINGS (Above which useful life may be impaired)

Storage Temperature	-25°C to +125°C
Operating Temperature (See curves)	-25°C to +70°C
CCD 145: Pins 2, 3, 4, 5, 8, 9, 10, 11, 12, 16, 18, 19, 20, 21, 22, 24, 27	-0.3V to 18V
Pin 26	0.0V to 1V
Pins 7, 14, 15, 28	-3.0V to 0V
Pins 1, 6, 13, 17, 23, 25	NC
Pins 23, 25	See caution note.

CAUTION NOTE:

These devices have limited built-in gate protection. It is recommended that static discharge be controlled and minimized. Care must be taken to avoid shorting pins $VIDEO_{OUT}$ and $COMP_{OUT}$ to V_{SS}, V_{CD} or V_{DD} during operation of the devices. Shorting these pins even temporarily may destroy output amplifiers.

DC CHARACTERISTICS: T_P = 25°C (Note 1)

		MAX	
V_{DD}	Output Amplifier Drain Supply Voltage	14.0	Note 2
I_{DD}	Output Amplifier Drain Supply Current	6.0	
V_{CD}	Compensation Amp. Drain Supply Voltage	14.0	Note 2
I_{CD}	Compensation Amp Drain Supply Current	6.0	
V_{PG}	Photogate Bias Voltage	6.0	
V_{RD}	Reset Drain Supply Voltage	12.5	
V_{OG}	Output Gate Bias Voltage	5.5	
V_{SINK}	Anti-Blooming Sink Voltage	14.0	
V_{BIAS}	Amplifier Bias Voltage	3.5	
V_{SG}	Amplifier Signal Ground	0.3	
V_{SS}	Substrate Ground	−2.0	Note 3

CLOCK CHARACTERISTICS: T_P = 25°C

			MAX	
ϕ_{1AL}, $V_{\phi 1BL}$ ϕ_{2AL}, $V_{\phi 2BL}$	Transport Clocks LOW			Notes 4, 5
ϕ_{1AH}, $V_{\phi 1BH}$ ϕ_{2AH}, $V_{\phi 2BH}$	Transport Clocks HIGH			Note 5
ϕ_{XAL}, $V_{\phi XBL}$	Transfer Clocks LOW			Notes 4, 5
ϕ_{XAH}, $V_{\phi XBH}$	Transfer Clocks HIGH			Note 5
$V_{\phi RL}$	Reset Clock LOW			Notes 4, 5
$V_{\phi RH}$	Reset Clock HIGH			Note 5
$V_{\phi SHL}$	Sample Clock LOW			Notes 4, 5
$V_{\phi SHH}$	Sample Clock HIGH			Notes 5, 6
$f_{\phi 1A}$, $f_{\phi 1B}$ $f_{\phi 2A}$, $f_{\phi 2B}$	Maximum Transport Clock Frequency			Notes 7, 8
$f_{\phi R}$	Maximum Reset Clock Frequency (Output Data Rate)			Notes 7, 8
t_R, t_F (ϕ_A, ϕ_{1A}, ϕ_{1B}, ϕ_{2B}, ϕ_{XA}, ϕ_{XB})	Transport and Transfer Clocks Rise and Fall Times	>20		
$V_{\phi ICAL}$, $V_{\phi ICBL}$	Integration Control Clocks LOW		5 to 7	Note 9
$V_{\phi ICAH}$, $V_{\phi ICBH}$	Integration Control Clocks HIGH		11.5	

AC CHARACTERTISTICS: T_P = 25°C, f_{data} = 2.5MHz, t_{int} = 1.0 ms, Light Source* = 2854°K + 2.0mm thick Schott BG-38 and OCLI WBHM Filters. All operating voltages nominal specified values. All tests done using "Test Load Configuration."

1500:1	
7500:1	
36	pJ/cm²
0.27	μJ/cm²
.99999	
5.0	V
85	mW
1	KΩ
0.8	mV

PERFORMANCE CHARACTERISTICS: T_P = 25°C, f_{data} = 2.5MHz, t_{int} = 1.0 mS, Light Source* = 2854°K + 2.0mm thick Schott BG-38 and OCLI WBHM filters. All operating voltages nominal specified values. Sample and Hold Clock is used.

MIN	TYP		UNIT	
	70	140	mV	
	50		mV	
	30		mV	
	40		mV	
	20		mV	
				Note 12
	1		mV	
	1		mV	
	1		mV	
	4.5		V/μJcm⁻²	
	1.2	2.0	V	Note 13

* OCLI WBHM = Optical Coating Laboratory, Inc. Wide Band Hot Mirror.

** All PRNU measurements are taken at an 700 mV output level using an f/5.0 lens and exclude the outputs from the first and last elements of the array. The "f" number is defined as the distance from the lens to the array divided by the diameter of the lens aperture. As the "f" number increases, the resulting more highly collimated light causes the package window imperfections to dominate and increase PRNU. A lower "f" number results in less collimated light causing device photosite blemishes to dominate the PRNU.

NOTES:

:k in good thermal contact with the entire backside of the device

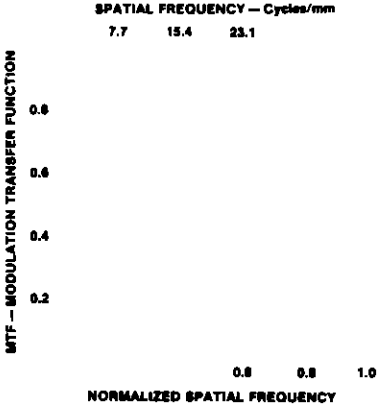
ss than 0.0V.
arge injection that results in an increase in apparent dark signal
ϕ_{SH} = 5pF.
cuitry. This is employed for the highest linearity. See output photographs

l8 and OCLI WBHM filters

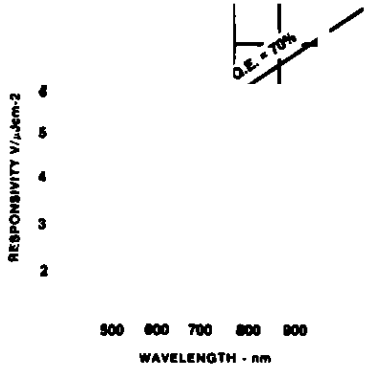
TYPICAL PERFORMANCE CURVES

MODULATION TRANSFER FUNCTIONS FOR TWO BROADBAND ILLUMINATION SOURCES

MODULATION TRANSFER FUNCTIONS FOR NARROW BAND ILLUMINATION SOURCES

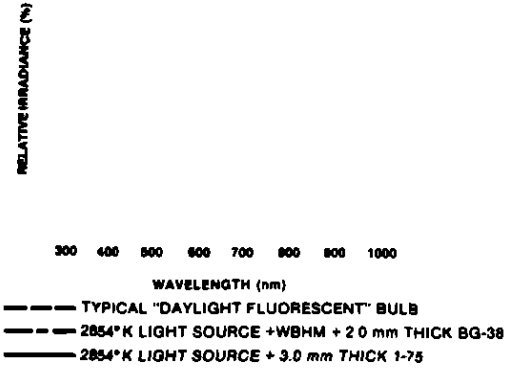


TYPICAL SPECTRAL RESPONSE

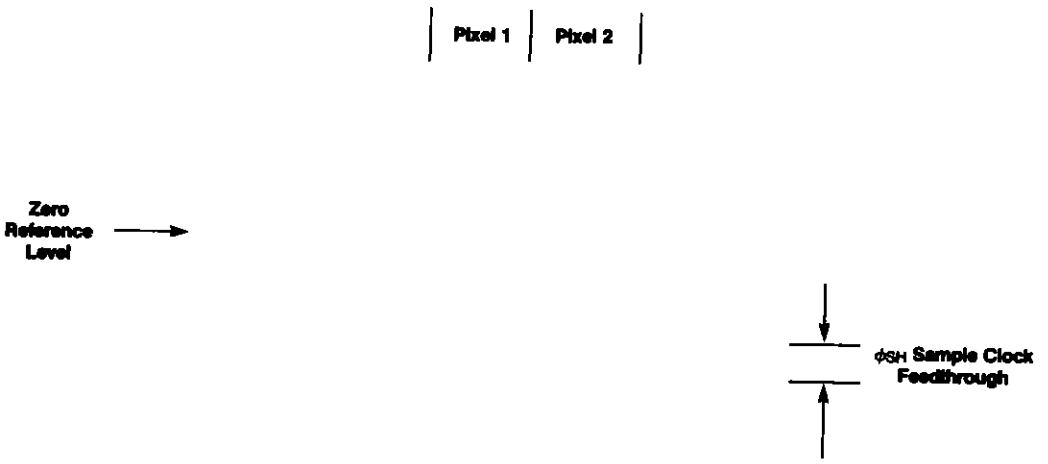


SINGLE-PIXEL DARK SIGNAL NON-UNIFORMITIES VERSUS INTEGRATION TIME

DC AND LOW-FREQUENCY DARK SIGNAL VS INTEGRATION TIME



FAIRCHILD CCD145 OUTPUT PHOTOGRAPHS



VOUT with ϕSH employed.

VOUT with ϕSH held high.

FIGURE 1: INTEGRATION CONTROL TIMING DIAGRAM

(Note 4)

NOTES:

1. $t_1 > (t_{fall}$ of $\phi x)$.
2. All charge generated in photosites during t_{IC} is dumped in V_{SINK}.
3. All charge generated in photosites < Q_{SAT} during t_{INT} is transferred into the shift registers during ϕx clock-high period. Photosite charge > Q_{SAT} (shift reg.) generated during t_{INT} goes into V_{SINK} if anti-blooming voltage is optimized.
4. ϕ_{IC} clock-low = 5 to 7 volts will give best anti-blooming operation.
5. ϕ_{IC} t_{rise} & $t_{fall} > 4\mu s$ to minimize clock coupling of ϕ_{EC} into V_{OUT}.
6. To eliminate integration control, but retain anti-blooming ϕ_{IC} = +5 VDC.
7. To eliminate both integration control and anti-blooming, ϕ_{IC} = 0VDC or V_{SS}(−2V).
8. To use integration control without anti-blooming, use ϕ_{IC} clock-low = 0.0 to 0.7 volts and ϕ_{IC} clock-high = same range as ϕ_T or ϕ_1 clock-high voltage.

FIGURE 2: MAXIMUM OUTPUT VOLTAGE vs. ϕ_{IC} VOLTAGE

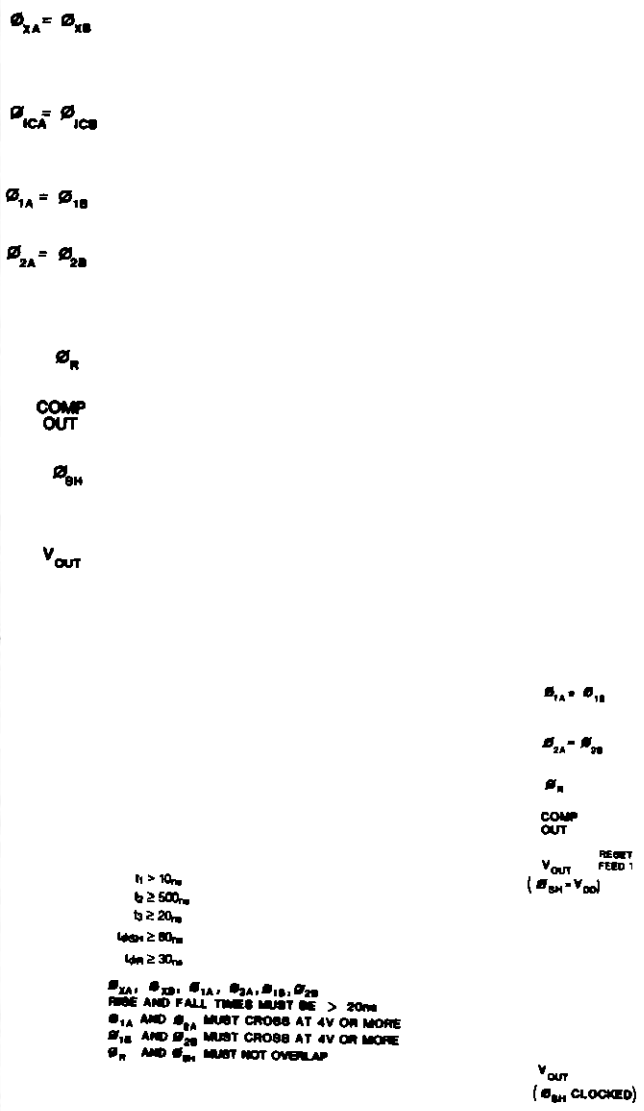
Perfect Anti-Blooming

Maximum Output Voltage

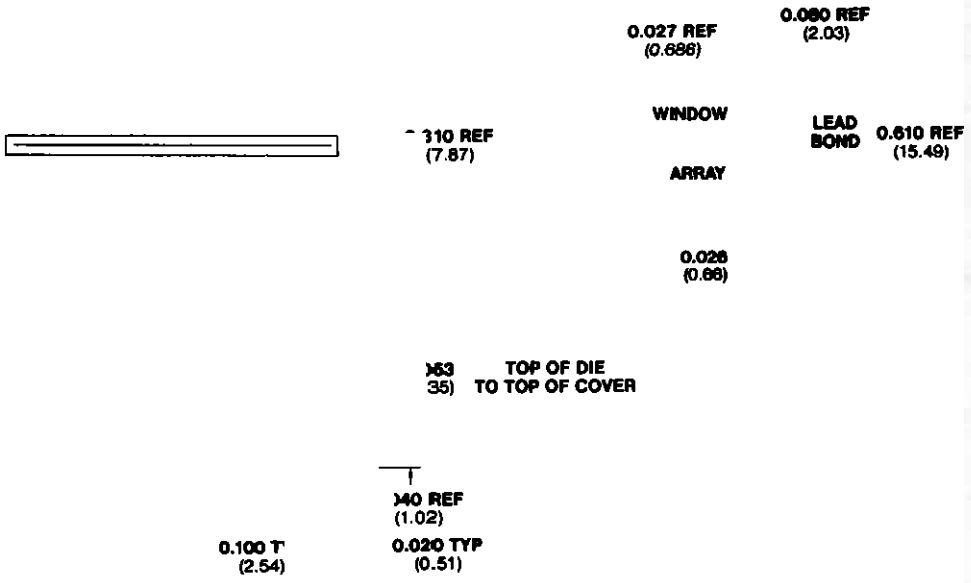
~5 to 7 volts

ϕ_{IC} Voltage (Volts DC or Volts at ϕ_{IC}-clock-low)

TIMING DIAGRAM



PACKAGE OUTLINE
28-Pin Dual In-line Ceramic Package



NOTES

All dimensions in inches (bold) and millimeters (parentheses). Header is black ceramic (Al_2O_3) Window is glass. The amplifier of the device is located near the notched end of the package.

DEVICE CARE AND OPERATION:

Glass may be cleaned by saturating a cotton swab in alcohol and lightly wiping the surface. Rinse off the alcohol with de-ionized water. Allow the glass to dry preferably by blowing with filtered dry N_2 or air.

It is important to note in design and applications considerations that the devices are very sensitive to thermal conditions. The dark signal DC and low frequency components approximately double for every 5° C temperature increase and single-pixel dark signal non-uniformities approximately double for every 8° C temperature increase. The devices may be cooled to achieve very long integration times and very low light level capability.

ORDER INFORMATION:

Order CCD145 DC where "D" stands for a ceramic package and "C" for commercial temperature range.

FAIRCHILD WESTON

CCD IMAGING DIVISION

CCD151
3456 – Element
Line Scan Image Sensor

FEATURES

- **Very high resolution: 3456 photosites**
- **Small element pitch: 7μm**
- **Low dark signal**
- **High responsivity**
- **Dynamic range typical: 2500:1**
- **Over 1 V peak-to-peak output**
- **Dark reference contained in sampled-and-held output**
- **Special selections available — consult factory.**

DESCRIPTION

The CCD151 is a 3456-element line image sensor designed for page scanning applications including facsimile, copier, optical character recognition and other imaging applications which require very high resolution, high sensitivity and moderate data rates.

The 3456 sensing elements of the CCD151 provide 400-line per inch resolution across an 8½ inch page which is double the international facsimile standard and satisfactory for many copier applications.

The photoelement size is 7μm (0.28 mils) by 7μm (0.28 mils) on 7μm (0.28 mils) centers. The device is manufactured using Fairchild Weston advanced charge-coupled device n-channel isoplanar buried-channel technology.

PIN NAMES	DESCRIPTION
V_{PG}	Photogate
ϕ_{XA}, ϕ_{XB}	Transfer Clocks
ϕ_{1A}, ϕ_{2A}	Transport Clocks
ϕ_{1B}, ϕ_{2B}	
V_{OG}	Output Gate
V_{OUT}	Video Output Terminal
V_{DD}	Output Amplifier Drain
V_{B1}	Output Amplifier Bias 1
V_{B2}	Output Amplifier Bias 2
ϕ_R	Reset Clock
ϕ_{SH}	Sample-and-Hold-Clock
V_{SG}	Signal Ground
V_{SS}	Substrate (Ground)
NC	No Connection
TP1, TP2	Test Points
TP3, TP4	
V_{PD}	Peripheral Diode

PIN CONNECTION DIAGRAM
(TOP VIEW)

NC	1	28	V_{SS}
ϕ_R	2	27	V_{SG}
V_{OG}	3	26	ϕ_{SH}
V_{PD}	4	25	V_{DD}
NC	5	24	V_{OUT}
NC	6	23	V_{B1}
NC	7	22	V_{B2}
ϕ_{2A}	8	21	ϕ_{2B}
ϕ_{1A}	9	20	ϕ_{1B}
ϕ_{XA}	10	19	ϕ_{XB}
TP3	11	18	TP1
TP4	12	17	TP2
V_{SS}	13	16	V_{PG}
V_{SS}	14	15	V_{SS}

Fairchild Weston Systems, Inc. CCD Imaging Division.
810 W. Maude Ave., Sunnyvale, California 94086
(408) 720-7600, TWX 910-373-2110

BLOCK DIAGRAM

ANALOG TRANSPORT SHIFT REGISTER A

ANALOG TRANSPORT SHIFT REGISTER B

O = CCD 151 PIN NUMBER
D = DARK REFERENCE CELL
I = ISOLATION CELL
N = 3486 FOR CCD 151

FUNCTIONAL DESCRIPTION

The CCD151 consists of the following functional elements illustrated in the Block Diagram:

Image Sensor Elements — A row of 3456 image sensor elements separated by a diffused channel stop and covered by a silicon dioxide surface passivation layer. Image photons pass through the transparent silicon dioxide layer and are absorbed in the single crystal silicon creating hole-electron pairs. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated in each photosite is a linear function of the incident illumination intensity and the integration period. The output signal will vary in an analog manner from a thermally generated background level at zero illumination to a maximum at saturation under bright illumination.

Two Transfer Gates — Gate structures adjacent to the row of image sensor elements. The charge packets accumulated in the image sensor elements are transferred out via the transfer gates to the transport registers whenever the transfer gate voltages go HIGH. Alternate charge packets are transferred to the A and B transport registers.

Two Analog Transport Shift Registers — One on each side of the line of image sensor elements and are separated from it by a transfer gate. The two registers, called the transport registers, are used to move the light generated charge packets delivered by the transfer gates serially to the charge detector/amplifier. The complimentary phase relationship of the last elements of the two transport registers provides for alternate delivery of charge packets to establish the original serial sequence of the line of video in the output circuit.

A Gated Charge Detector/Amplifier — Charge packets are transported to a precharged diode whose potential changes linearly in response to the quantity of the signal charge delivered. This potential is applied to the gate of the output n-channel MOS transistor producing a signal at the output V_{OUT}. A reset transistor is driven by the reset clock (ϕ_R) and recharges the charge detector diode capacitance before the arrival of each new signal charge packet from the transport registers.

Transport Clocks ϕ_{1A}, ϕ_{2A}, ϕ_{1B}, ϕ_{2B} — The two sets of 2-phase waveforms applied to the gates of the transport registers to move the charge packets received from the image sensor elements to the gated charge detector/amplifier.

Sample-and-Hold Clock ϕ_{SH} — The voltage waveform applied to the sample-and-hold gate in the output amplifier to create a continuous sampled video signal at the output. The sample-and-hold feature may be defeated by connecting ϕ_{SH} to V_{DD}.

Reset Clock ϕ_R — The voltage waveform required to reset the voltage on the charge detector.

Dark Reference Circuitry — Eight additional sensing elements at both ends of the array are covered by opaque metalization. They provide a dark (no illumination) signal reference which is delivered at both ends of the line of video output representing the illuminated sensor elements (labeled "D" in the Block Diagram). These reference levels are useful as inputs to external dc restoration circuitry.

Peripheral Diode — Serves to reduce peripheral electron noise in the inner shift registers.

DEFINITION OF TERMS

Pixel — A picture element (photosite).

Transfer Clocks ϕ_{XA}, ϕ_{XB} — The voltage waveforms applied to the transfer gates to move the accumulated charge from the image sensor elements to the CCD transport registers.

Dark Reference — Video output level generated from sensing elements covered with opaque metalization which provides a reference voltage equivalent to device operation in the dark. This permits use of external dc restoration circuitry.

Isolation Cell — This is a site on-chip producing an element in the video output that serves as a buffer between valid video data and dark reference signals. The output from an isolation cell contains no valid video information and should be ignored.

RMS Noise Equivalent Exposure — The exposure level that gives an output signal equal to the rms noise level at the output in the dark.

Saturation Exposure — The minimum exposure level that will provide a saturation output signal. Exposure is equal to the light intensity times the photosite integration time.

Charge Transfer Efficiency — Percentage of valid charge information that is transferred between each successive stage of the transport registers.

Spectral Response Range — The spectral band in which the response per unit of radiant power is more than 10% of the peak response.

Responsivity — The output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure.

Total Photoresponse Non-uniformity — The difference of the response levels of the most and the least sensitive elements under uniform illumination. Measurement of PRNU excludes first and last elements.

Dark Signal — The output signal in the dark caused by thermally generated electrons that is a linear function of the integration time and highly sensitive to temperature.

Saturation Output Voltage — The maximum useable signal output voltage. Charge transfer efficiency decreases sharply when the saturation output voltage is exceeded.

Integration Time — The time interval between the falling edges of any two transfer pulses ϕ_{XA} or ϕ_{XB} as shown in the timing diagram. The integration time is the time between transfers of signal charge from the photosites into the transport registers.

TEST LOAD CONFIGURATION

CCD151

V_{OUT}

V_{B_2}

ABSOLUTE MAXIMUM RATINGS (Above which useful life may be impaired)

Storage Temperature	−25°C to +125°C
Operating Temperature	−25°C to +70°C
Pins 2, 3, 4, 8, 9, 10, 11, 12, 17, 18, 19, 20, 21, 22, 23, 25, 26, 27	*−0.3V to 18V*
Pin 16	−0.3V to 16V
Pins 13, 14, 15, 28	0V
Pins 1, 5, 6, 7 (See Caution Note)	NC
Pin 24 (See Caution Note)	Video Output

CAUTION NOTE:
to avoid shorting V_{OUT}, V_{SS}, or V_{DD} during operation of these devices. Shorting these pins even minimized. Care must be taken may destroy the output amplifiers.

Do not connect anything to a pin marked NC. They may be internally connected.

DC

CL

$V_{\Phi 1AL}$, $V_{\Phi 1BL}$ $V_{\Phi 2AL}$, $V_{\Phi 2BL}$	0.6
$V_{\Phi 1AH}$, $V_{\Phi 1BH}$ $V_{\Phi 2AH}$, $V_{\Phi 2BH}$	
$V_{\Phi XAL}$, $V_{\Phi XBL}$	
$V_{\Phi XAH}$, $V_{\Phi XBH}$	
$V_{\Phi RL}$	
$V_{\Phi RH}$	
$V_{\Phi SHL}$	
$V_{\Phi SHH}$	
$f_{DATA\ MAX}$	Frequency (Output Data Rate)

AC CHARACTERISTICS: T_p = 25° C, f_{clk} = 1.0MHz, t_{int} = 4ms, Light Source = 2854° K + 2.0mm thick Schott BG-38 and OCLI WBHM filters.* All operating voltages nominal specified values. (Note 1) All tests done using "Test Load Configuration."

	Dynamic Range (relative to rms noise) (relative to peak-to-peak noise)	 2500:1 500:1		
NEE	RMS Noise Equivalent Exposure	 .0001		$\mu J/cm^2$
SE	Saturation Exposure	.360		$\mu J/cm^2$
CTE	Charge Transfer Efficiency	.99999		
V_o	Output DC Level	5.5		V
P	Power Dissipation	75		mW
Z	Output Impedance	1.5		kΩ
N	Peak-to-Peak Noise	4		mV

PERFORMANCE CHARACTERISTICS: T_p = 25° C, f_{clk} = 1.0MHz, t_{int} = 4ms, Light Source = 2854° K + 2.0mm thick Schott BG-38 and OCLI WBHM filters.* All operating voltages nominal specified values. (Note 1)

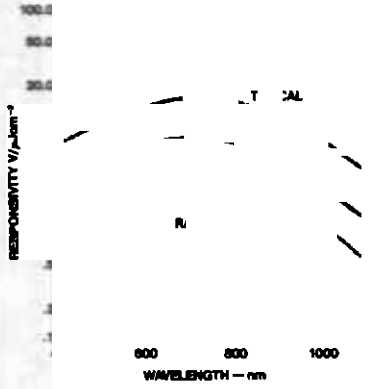
	CHARACTERISTICS			
PRNU**	Photoresponse Non-uniformity			
	Peak-to-Peak	120		mV
	Peak-to-Peak without Single-Pixel Positive and Negative Pulses	80		mV
	Single-pixel Positive Pulses	70		mV
	Single-pixel Negative Pulses	100		mV
	Register Imbalance ("Odd"/"Even")	20		mV
DS	Dark Signal			
	DC Component	.5	2	mV
	Low Frequency Component	.5	5	mV
SPDSNU	Single-pixel DS Non-uniformity	3	8	mV
R	Responsivity	4.0	9	Volts per $\mu J/cm^2$
V_{SAT}	Saturation Output Voltage	1800	3000	mV

*OCLI WBHM = Optical Coating Laboratory, Inc Wide Band Hot Mirror

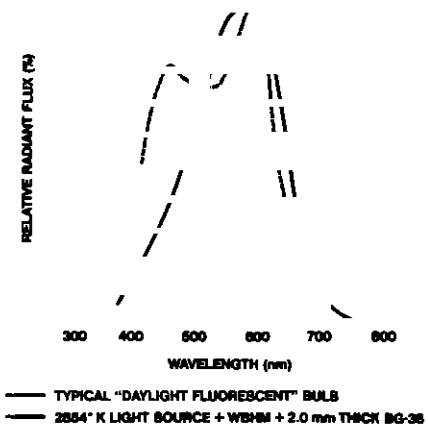
**All PRNU measurements are taken at an 800mV output level using an f/5.0 lens and exclude the outputs from the first and last elements of the array. The "f" number is defined as the distance from the lens to the array divided by the diameter of the lens aperture. As the "f" number increases, the resulting more highly collimated light causes the package window imperfections to dominate and increase PRNU. A lower "f" number results in less collimated light causing device photosite blemishes to dominate the PRNU.

TYPICAL PERFORMANCE CURVES

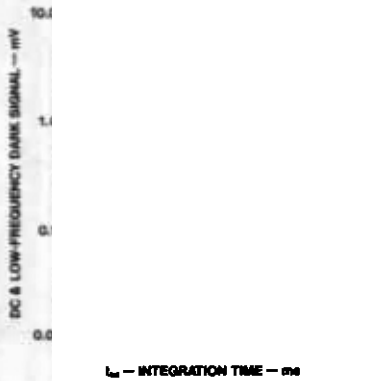
TYPICAL SPECTRAL RESPONSE



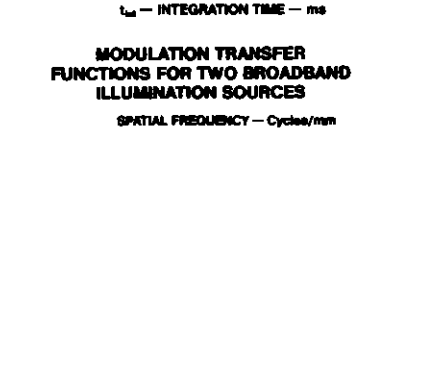
RELATIVE IRRADIANCE VERSUS WAVELENGTH



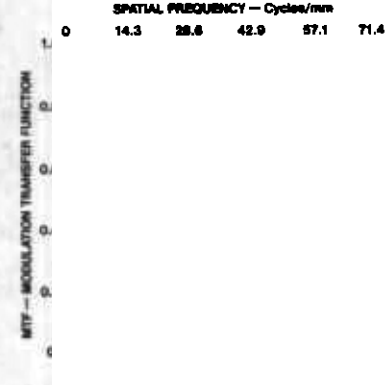
DC AND LOW-FREQUENCY DARK SIGNAL VERSUS INTEGRATION TIME



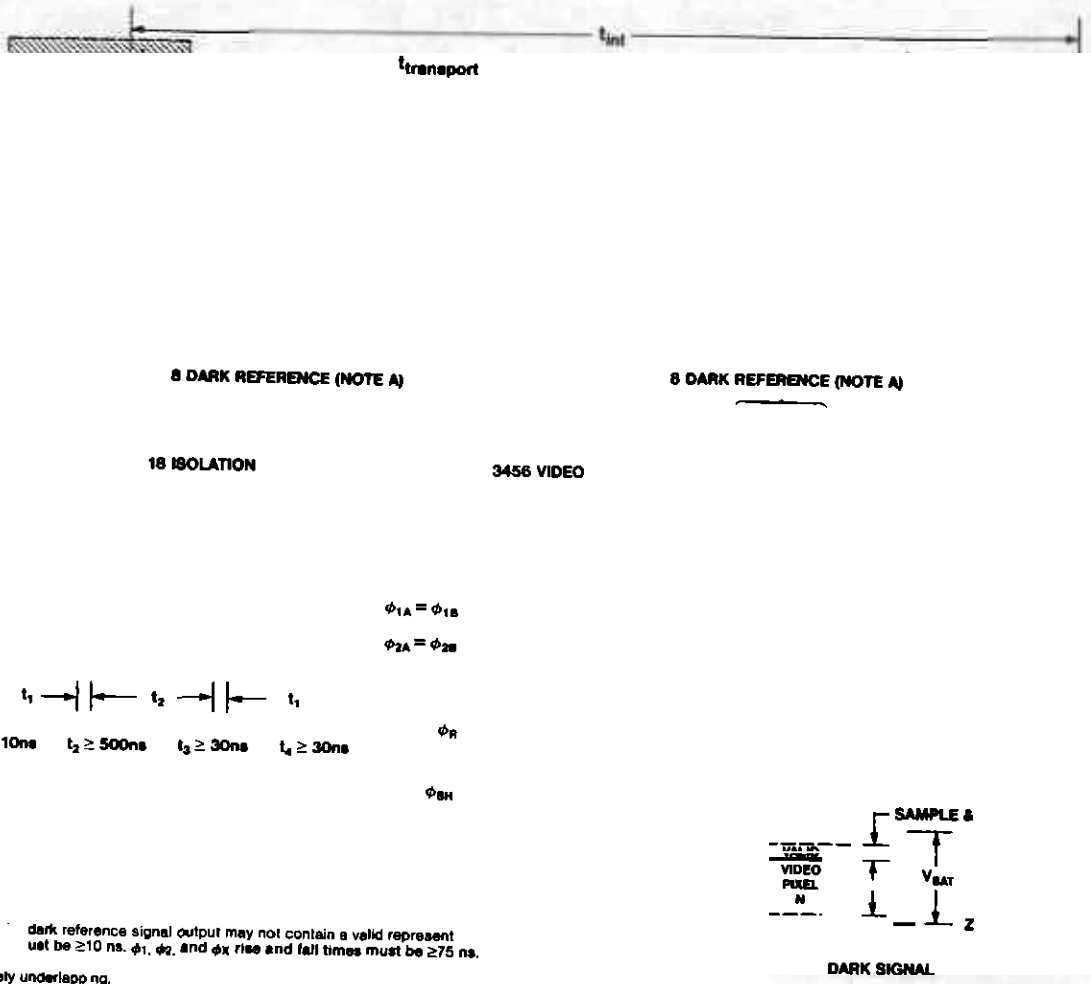
SINGLE-PIXEL DARK SIGNAL NON-UNIFORMITIES VERSUS INTEGRATION TIME



MODULATION TRANSFER FUNCTIONS FOR NARROW BAND ILLUMINATION SOURCES

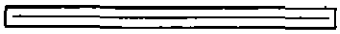


MODULATION TRANSFER FUNCTIONS FOR TWO BROADBAND ILLUMINATION SOURCES



A. The first and last [illegible] dark reference signal output may not contain a valid represent
B. uet be ≥10 ns. ϕ_1, ϕ_2, and ϕ_X rise and fall times must be ≥75 ns.
C.
D. ϕ_R and ϕ_{SH} must be completely underlapp ng.
E. ϕ_R must occur entirely within the high time of the high ϕ_1 or ϕ_2 clock ϕ_{SH} must occur entirely within the low time of the other transport clock

PACKAGE OUTLINE
28-Pin Dual In-line Ceramic Package



NOTES

All dimensions in inches (bold) and millimeters (parentheses). Header is black ceramic (Al_2O_3). Window is glass. The amplifier of the device is located near the notched end of the package.

DEVICE CARE AND OPERATION

Glass may be cleaned by saturating a cotton swab in alcohol and lightly wiping the surface. Rinse off the alcohol with de-ionized water. Allow the glass to dry preferably by blowing with filtered dry N_2 or air.

It is important to note in design and applications considerations that the devices are very sensitive to thermal conditions. The dark signal DC and low frequency components approximately double for every 5°C temperature increase and single-pixel dark signal non-uniformities approximately double for every 12°C temperature increase. The devices may be cooled to achieve very long integration times and very low light level capability.

ORDER INFORMATION

Order CCD151 DC where "D" stands for a ceramic package and "C" for commercial temperature range.

Also available separately is a printed circuit board that includes all the necessary clocks, logic drivers and video amplifiers to operate the CCD151DC. The board is fully assembled and tested and requires only one power supply for operation (+20V). The printed circuit board order code is: CCD151DB.

Description	Device Type Order Code
CCD151 3456 × 1 Line Image Sensor	CCD151DC
Design Development Board for CCD151	CCD151DB

FAIRCHILD WESTON

CCD IMAGING DIVISION

CCD153A
512-Element High-Speed Linear Image Sensor

FEATURES

- 512 × 1 photosite array
- 13μm × 13μm photosites on 13μm pitch
- High speed: up to 20 MHz data rate
- Enhanced spectral response
- Low dark signal
- High responsivity
- On-chip clock drivers
- Dynamic range typical: 5000:1
- Over 1 V peak-to-peak outputs
- Dark and white references contained in sample-and-hold outputs

DESCRIPTION

153A (512 pixels) are
el counts and capaci-

13 μm (0.51mils) on
s are manufactured
d-generation charge-
silicon-gate buried-

PIN NAMES	DESCRIPTION
$VOUT_A$	
ϕSH_{GA}	
ϕSH_{CA}	
V_{CD}	
NC	
V_T	
V_{EI}	
V_{SS}	
V_{PG}	
ϕX	
ϕT	
V_{RD}	
ϕSH_{CB}	
ϕSH_{GB}	
$VOUT_B$	
V_{DD}	

PIN CONNECTION DIAGRAM (TOP VIEW)

$VIDEOOUT_A$	1	24	**V_{DD}**
ϕSH_{GA}	2	23	**$VIDEOOUT_B$**
ϕSH_{CA}	3	22	**ϕSH_{GB}**
V_{CD}	4	21	**ϕSH_{CB}**
NC	5	20	**NC**
NC	6	19	**NC**
NC	7	18	**V_{RD}**
V_{CD}	8	17	**V_T**
NC	9	16	**ϕT**
	10	15	**ϕX**
	11	14	**V_{PG}**
	12	13	**V_{SS}**

Fairchild Weston Systems, Inc. CCD Imaging Division.
810 W. Maude Ave., Sunnyvale, California 94086
408-720-7600, TWX 910-373-2110

Fig. 1 BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION

The CCD 153A consists of the following functional elements illustrated in the Block Diagram and Circuit Diagram (Fig. 1).

Photosites: A row of 512 image sensor elements separated by a diffused channel stop and covered by a silicon dioxide surface passivation layer. Image photons pass through the transparent silicon creating hole-electron pairs. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated in each photosite is a linear function of the incident illumination intensity and the integration period. The output signal will vary in an analog manner from a thermally generated background level at zero illumination to a maximum at saturation under bright illumination.

Photogate: The photogate structure, located at the edge of the photosites, provides a bias voltage for the photosites.

Transfer Gate: The transfer gate structure separates the outer edge of the photogates from the analog shift registers. Charge-packets generated and accumulated in the photosites are transferred into the transport analog shift registers whenever the transfer gate voltage goes "High." All odd-numbered charge packets are transferred into the "A" transport analog shift register; all even-numbered charge packets are transferred into the "B" transport analog shift register. The transfer gate also controls the input of charge from V_{EI} into the white reference cells (described below) The time interval between successive transfer pulses determines the integration time

Analog Shift Registers: Four 273-element analog shift registers transport charge towards the output end of the chip. The two inner registers, the transport registers, move the image-generated charge packets serially to the two gated charge detectors and amplifiers. The two outer shift registers, the peripheral registers, accumulate charge generated at the chip periphery (by photons passing through unavoidable gaps in the light shield layer, etc) and transport it to charge sinks The primary shift register clock is ϕ_T. The complementary phase relationship of the secondary shift register clocks $\overline{\phi_T}$ and $\overline{\overline{\phi_T}}$, generated on-chip, provide alternate delivery of charge packets from "A" and "B" shift registers to their amplifiers so that the original serial sequential string of video information may be easily demultiplexed off-chip

Gated Charge Detectors & Reset Gates: Each transport analog shift register delivers charge packets to a precharged diode. The change in diode potential is linearly proportional to the amount of charge delivered in the charge packet. This potential is applied to the input gate of a MOS transistor amplifier (see below), which linearly amplifies the input potential. The diode is reset to the reset drain bias voltage (V_{RD}) by the reset gate structure. Reset occurs when both the internal reset clocks ($\overline{\phi_T}$ on the "A" side, $\overline{\phi_T}$ on the "B" side) are "High." Each side is reset just before the next charge packet is delivered from its respective transport analog shift register

Output Amplifiers and Sample-and-Hold Gates: Each sides' gated charge integrator drives the input of a two-stage linear MOS-transistor amplifier. A schematic diagram of this circuit is shown in Figure 9 below The two stages of each amplifier are separated by sample-and-hold gates. The output of the first stage is connected to the input of the second stage whenever the sample-and-hold gate is "High " The output of the second stage is connected to the VIDEOOUT pin. The sample-and-hold gates are switching MOS transistors: clocking these gates results in a sampled-and-held output, thus eliminating the reset clock feedthrough. When on-chip sample-and-hold is used, pin 2 is to be tied to pin 3 and pin 21 is to be tied to pin 22. Off-chip sample-and-hold pulses can be supplied through pins 2 and 22. The sample-and-hold operation can be disabled by tying pins 2 and 22 to V_{DD}. Whenever on-chip sample-and-hold is not used, pins 3 and 21 should be left unconnected.

Clock Driver Circuits: Two MOSFET clock-driver circuits on-chip allow sample-and-held operation of the CCD153A with only two externally-supplied clocks: the square-wave primary shift register transport clock ϕ_T, which determines the output data rate, and the transfer clock ϕ_X, which determines the integration time.

Dark and White Reference Cells and Circuitry: At each end of the 512-photosite array there are four additional sensing elements covered by opaque metallization. These "Dark

Fig. 2 TEST LOAD CONFIGURATION

DEFINITION OF TERMS

Charge-Coupled Device—A charge-coupled device is a semiconductor device in which finite isolated charge-packets are transported from one position in the semiconductor to an adjacent position by sequential clocking of an array of gates. The charge-packets are minority carriers with respect to the semiconductor substrate.

Transfer Clock ϕ_X—The transfer clock is the voltage waveform applied to the transfer gate to move the accumulated charge from the image sensor elements to the CCD transport shift registers.

Transport Clock ϕ_T—The transport clock is the clock applied to the gates of the CCD transport shift registers to move the charge-packets received from the image sensor elements to the gated charge-detector/amplifiers.

Sample-and-Hold Clock (ϕ_{SHA}, ϕ_{SHB})—The voltage waveform applied to the sample-and-hold gates in the output amplifiers to create a continuous sampled video signal at the output. The sample-and-hold feature may be defeated by connecting $\phi_{SH(A+B)}$ to V_{DD}.

Isolation Cell—A site on-chip producing an element in the video output that serves as a buffer between valid video data and dark reference signals. The output from an isolation cell contains no valid information and should be ignored.

Dynamic Range—The saturation exposure divided by the rms temporal noise equivalent exposure. Dynamic range is sometimes defined in terms of peak-to-peak noise. To compare the two definitions a factor of four to six is generally appropriate in that peak-to-peak noise is approximately equal to four to six times rms noise.

RMS Noise Equivalent Exposure—The exposure level that gives an output signal equal to the rms noise level at the output in the dark.

Saturation Exposure—The minimum exposure level that will provide a saturation output signal. Exposure is equal to the light intensity times the photosite integration time.

Charge Transfer Efficiency—Percentage of valid charge information that is transferred between each successive stage of the transport registers.

Responsivity—The output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure.

Total Photoresponse Non-uniformity—The difference of the response levels of the most and the least sensitive element under uniform illumination. Measurement of PRNU excludes first and last elements.

Dark Signal—The output signal in the dark caused by thermally generated electrons that is a linear function of the integration time and highly sensitive to temperature. (See accompanying photos for details of definition.)

Saturation Output Voltage—The maximum useable signal output voltage. Charge transfer efficiency decreases sharply when the saturation output voltage is exceeded.

Integration Time—The time interval between the falling edge of any two successive transfer pulses (ϕ_X). The integration time is the time allowed for the photosites to collect charge.

Pixel—A picture element (photosite).

PHOTOELEMENT DIMENSIONS

All dimensions are typical values.

ABSOLUTE MAXIMUM RATINGS (Above which useful life may be impaired)

Storage Temperature
Operating Temperature (See Curves)
CCD153A Pins 2, 3, 4, 8, 11, 12, 14, 15, 16, 17, 18, 21, 22, 24
Pin 13
Pins 5, 6, 7, 9, 10, 19, 20
Pins 1, 23

CAUTION NOTE: These devices have limited built-in gate protection. It is recommended that static discharge be controlled and minimized. Care must be taken to avoid shorting pins V_{OUT} A&B to V_{SS} or V_{DD} during operation of these devices. Shorting these pins temporarily to V_{SS} or V_{DD} may destroy the output amplifiers.

D

V_{CD}	Clock Driver Drain Supply Voltage	13 5	
I_{CD}	Clock Driver Drain Supply Current		
		13.5	
		8.5	
	DC Electrode Bias Voltage	5 5	
	Electrical Input Bias Voltage		
V_{SS}	Substrate (Ground)		
V_{RD}	Reset Drain Supply		

(

$V_{\phi XL}$, $V_{\phi TL}$			0.3
$V_{\phi XH}$, $V_{\phi 1r}$,	Transfer & Transport Clock HIGH		
$f_{DATA\ MAX}$	Maximum Output Data Rate	12	

NOTES:

1. T_P is defined as the package temperature, measured on a copper block in good thermal contact with the entire backside of the package.
2. ALL V_{SS} pins must be grounded. All NC pins must be left unconnected.
3. V_{DD} pins may be connected to V_{CD} and/or V_{RD} pins
4. $V_T = 0.55\ \phi x_{HIGH} = 0.55\ \phi T_{HIGH}$
5. V_{EI} is used to generate the white reference output. These two signals can be eliminated by connecting V_{EI} to V_{DD}.
6. Negative transients on any clock pin going below 0 0 volts may cause charge injection, which results in an increase in apparent DS.
7. C ϕT = 180 pF; C ϕX = 50 pF.
   All clock rise and fall times should be > 30ns.
8. The minimum clock frequency is limited by increases in dark signal
9. $f_{DATA} = 2\ (f\ \phi T)$
10. OCLI WBHM = Optical Coating Laboratory, Inc. Wide Band Hot Mirror.
11. CTE is the measurement for a one-stage transfer.
12. See photographs for PRNU definitions.
13. Video mismatch is the difference in ac amplitudes between $V_{OUT\ A}$ and $V_{OUT\ B}$ under uniform illumination by attenuation/amplification of one of the video outputs.
14. DC mismatch is the difference in dc output level V_O between $V_{OUT\ A}$ and $V_{OUT\ B}$.
15. See photographs for dark signal definitions.
16. Dark signal component approximately doubles for every 5-10 °C in T_P.
17. Each SPDSNU is measured from the DS level adjacent to the base of the SPDSNU. The SPDSNU approximately doubles for every 5-15 °C in T_P.
18. V_{RD} voltages in the lower range improves amplifier linearity.

AC CHARACTERTISTICS: (Note 1)
T_P = 25°C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms, Light Source* = 2854°K + 2.0 mm thick
Schott BG-38 and OCLI WBHM filters.
All operating voltages nominal specified values. All tests done using "Test Load Configuration."

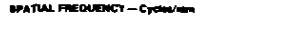
Dynamic Range (relative to peak-to-peak noise)		0.00009	
(relative to rms noise)		0.67	μj/cm2
		0.99999	
		1.5	
		100	
		1.5	

OCLI WBHM = Optical Coating Laboratory, Inc. Wide Band Hot Mirror
PRNU measurements include both register outputs but exclude the outputs from the first and last elements of the array. Also excluded from the measurement are video and dc mismatch.
All PRNU measurements are taken at a 600 mV output level using an f/5.0 lens.
The "f" number is defined as the distance from the lens to the array divided by the diameter of the lens aperture. As the "f" number increases, the resulting more highly collimated light causes the package window imperfections to dominate and increase PRNU. A lower "f" number results in less collimated light causing device photosite blemishes to dominate the PRNU.

Fig. 3 TEST LOAD CONFIGURATION

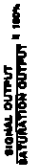
TYPICAL PERFORMANCE CURVES

MODULATION TRANSFER FUNCTIONS FOR TWO BROADBAND ILLUMINATION SOURCES



MODULATION TRANSFER FUNCTIONS FOR NARROW BAND ILLUMINATION SOURCES

OUTPUT SIGNAL LEVEL VERSUS INTEGRATION TIME 2854°K TUNGSTEN SOURCE WITH BG-38 AND WBHM FILTERS



SINGLE-PIXEL DARK SIGNAL NON-UNIFORMITIES VERSUS INTEGRATION TIME

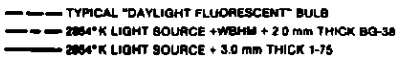
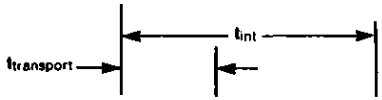


Fig. 4 PHOTORESPONSE NON-UNIFORMITY PARAMETERS (PRNU)



Zero Reference Level ≈ 800 mV Output A Voltage

Zero Reference Level ≈ 800 mV Output B Voltage

Peak-to-Peak Wilhout Single-Pixel Positive and Negative Rises

TEST CONDITIONS
T_P = +25°C. f_{DATA} = 1.25 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Light source = 2854°K tungsten + 2.0 mm thick Schott BG-38 and OCLI WBHM filters. PRNU measurements taken at an output voltage of ≈ 800 mV. Output fed through 5 MHz low pass filter.

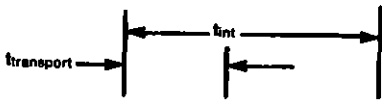
Fig. 5 PHOTORESPONSE NON-UNIFORMITY PARAMETERS (PRNU)

TEST CONDITIONS
T_P = +25°C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Light source = 2854°K tungsten +2.0 mm thick Schott BG-38 and OCLI WBHM filters. PRNU measurements taken at an output voltage of = 800 mV. Output fed through 5 MHz low pass filter.

Fig. 6 DARK SIGNAL PARAMETERS (DS)

TEST CONDITIONS
T_P = +25°C, f_{DATA} = 5 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Output fed through 5 MHz low pass filter.

Fig. 6 DARK SIGNAL PARAMETERS (DS)



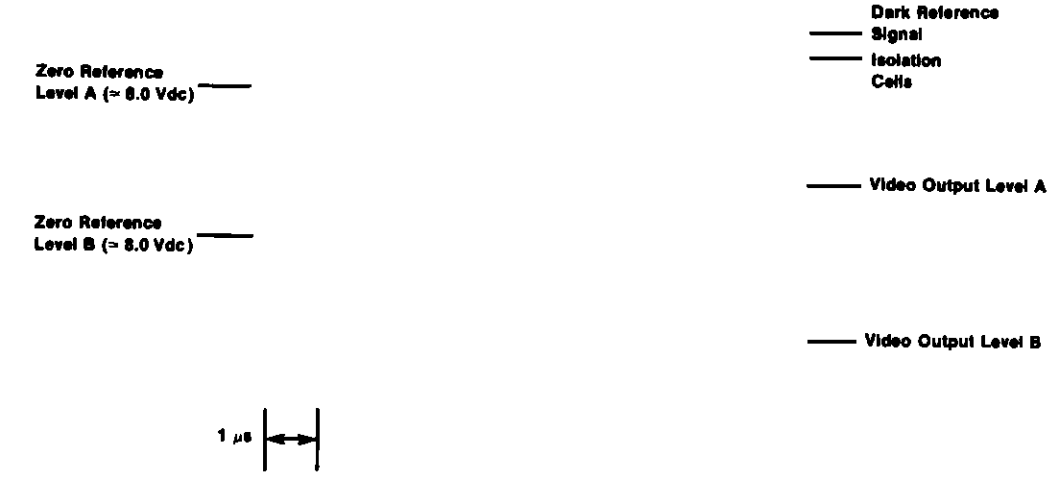
5 n

Zero Reference

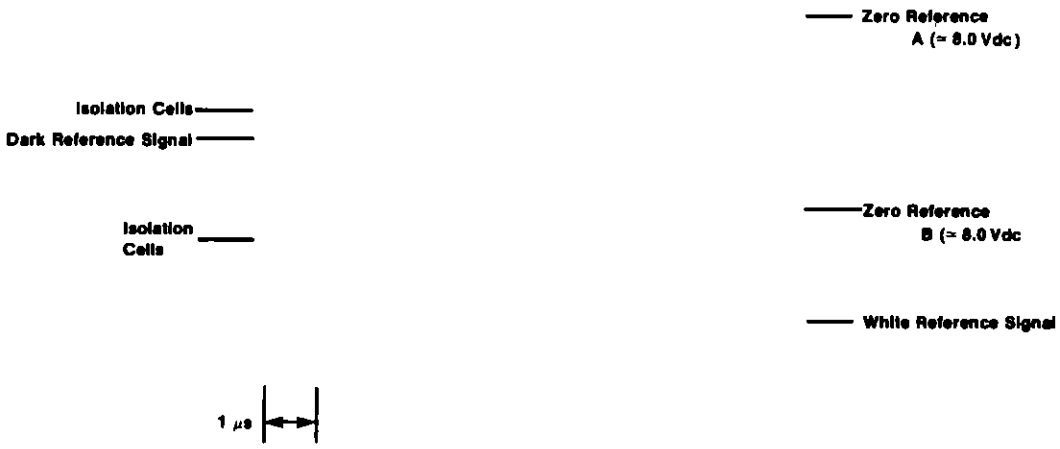
5 mV

TEST CONDITIONS
T_P = +25°C, f_{DATA} =1.25 MHz, t_{INT} = 1.0 ms. All voltages nominal specified values. fed through 5 MHz low pass filter.

Fig. 7 VIDEO OUTPUT TIMING PHOTOGRAPHS



Start of One Scan Video Output



End of One Scan Video Output

TEST CONDITIONS
T_P = +25° C, f_{DATA} = 5 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Light source = 2854° K tungsten with 2.0 mm thick Schott BG-38 and OCLI WBHM filters. Output fed through 5 MHz low pass filter.

Fig. 8 TIMING DIAGRAM

DEVICE CARE AND OPERATION

Glass may be cleaned by saturating a cotton swab in alcohol and lightly wiping the surface. Rinse off the alcohol with deionized water. Allow the glass to dry, preferably by blowing with filtered dry

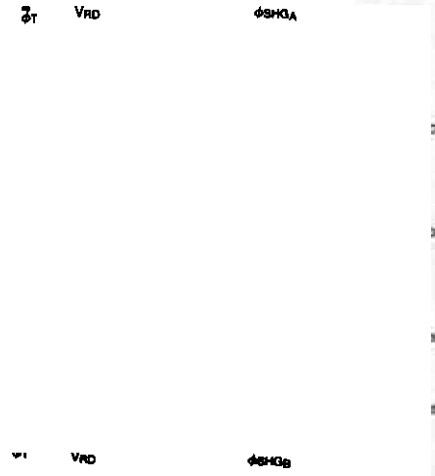
It is important t
ations that the de
The dark signal
mately double fc
pixel dark signa
every 8°C temp
to achieve very l
capability.

ORDER INFORI

Order CCD153A
and "C" for com

Also available a
necessary clock
the CCD153A. T
require only on
printed circuit
CCD153A, 143A
printed circuit bc
are to be placec
printed circuit bc

Fig. 9 OUTPUT AMPLIFIER SCHEMATIC



NOTE: $\bar{\phi}_T$ AND $\bar{\bar{\phi}}_T$ ARE INTERNALLY GENERATED RESET CLOCKS.

All dimensions in inches (**bold**) and millimeters (parentheses). Header is black ceramic (Al_2O_3). Window is glass. *The amplifier of the device is located near the notched end of* the package

FAIRCHILD WESTON

CCD IMAGING DIVISION

PRELIMINARY

CCD181
Variable-Element High-Speed Linear Image Sensor

FEATURES

- 2592 × 1 photosite array
- 10μm × 10μm photosites on 10μm pitch
- Anti-blooming and integration control
- Voltage-selectable array lengths:
  - 2592 elements 2048 elements
  - 1728 elements 1024 elements
- Enhanced spectral response (particularly in the blue region)
- Excellent low-light-level performance
- Low dark signal
- High responsivity
- High-speed operation
- Dynamic range typical: 7500:1
- Over 1V peak-to-peak outputs
- Dark references contained in sampled-and-held outputs
- Special selection available — consult factory

PIN NAME	DESCRIPTION
V_{SG}	Amplifier Signal Ground
V_{OUT_A}	Output Amplifier A Source
ϕSH_A	Sample and Hold Gate A
ϕR_A	Reset Gate A
V_{RD_A}	Reset Drain A
V_{BIAS_A}	Output Amplifier A Bias
V_{OG_A}	Output Gate A
ϕX	Transfer Clock
$\phi 2_A$, $\phi 2_B$	Transport Clocks
$\phi 1_A$, $\phi 1_B$	Transport Clocks
ϕIC	Integration Control Clock
V_{PG}	Photogate
V_{1728}	1728 Active Pixels Switch
V_{SS}	Substrate Ground
V_{1024}	1024 Active Pixels Switch
V_{2048}	2048 Active Pixels Switch
V_{SINK}	Anti-Blooming Control Sink
V_{OG_B}	Output Gate B
V_{BIAS_B}	Amplifier B Bias
V_{RD_B}	Output Amplifier B Bias
ϕR_B	Reset Gate B
ϕSH_B	Sample and Hold Gate B
V_{OUT_B}	Output Amplifier B Source
V_{DD}	Output Amplifier Drain

PIN CONNECTION DIAGRAM
(TOP VIEW)

V_{SG}	1	28	SS
V_{OUT_A}	2	27	DD
ϕSH_A	3	26	OUT_B
ϕR_A	4	25	SH_B
V_{RD_A}	5	24	R_B
V_{BIAS_A}	6	23	RD_B
V_{OG_A}	7	22	$BIAS_B$
ϕX	8	21	OG_B
$\phi 2_A$	9	20	2_B
$\phi 1_A$	10	19	1_B
ϕIC	11	18	SINK
V_{PG}	12	17	2048
V_{1728}	13	16	1024
V_{SS}	14	15	SS

Fairchild Weston Systems, Inc. CCD Imaging Division
810 W. Maude Ave., Sunnyvale, California 94086
(408) 720-7600, TWX 910-373-2110

GENERAL DESCRIPTION

The CCD181 is a 2592-element line image sensor designed for industrial measurement, telecine, and document scanning applications which require high resolution, high sensitivity and high data rate The incorporation of on-chip blooming and exposure controls allow the CCD181 to be extremely useful in an industrial measurement and control environment or environments where lighting conditions are difficult to control.

The CCD181 is equipped with special gates which allow the user to select 4 effective array lengths:

2592 elements: 300-lines/inch across 8.5 inch wide document
2048 elements: 240-lines/inch across 8.5 inch wide document
1728 elements: 200-lines/inch across 8.5 inch wide document
1024 elements: 120-lines/inch

The CCD181 is a third generation device having an overall improved performance compared with first and second generation devices, including enhanced blue response, excellent low light level performance, and high-speed operation up to 18 MHz.

The photoelement size is 10μm (0.39 mils) x 10μm (0.39 mils) on 10μm (0.39 mils) centers The device is manufactured using Fairchild Weston advanced charge-coupled device n-channel isoplanar buried-channel technology.

FUNCTIONAL DESCRIPTION

The CCD181 consists of the following functional elements illustrated in the block diagram and circuit diagram (see Fig 1A).

Photosites — A row of 2592 image sensor elements separated by a diffused channel stop and covered by a silicon dioxide surface passivation layer. Image photons pass through the transparent silicon creating hole-electron pairs. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated in each photosite is a linear function of the incident illumination intensity and the integration period. The output signal will vary in an analog manner from a thermally generated background level at zero illumination to a maximum at saturation under bright illumination.

Two Transfer Gates — Gate structures adjacent to the row of image sensor elements. The charge packets accumulated in the photosites are transferred in parallel via the transfer gates (ϕX) to the transport shift registers whenever the transfer gate voltages go high. Alternate charge packets are transferred to the A and B transport registers

Two Analog Transport Shift Registers — The transport shift registers are used to move the light generated charge packets delivered by the transfer gates (ϕ1A, ϕ1B, ϕ2A, ϕ2B) serially to the charge detector/amplifier The complementary phase relationship of the last elements of the two transport registers provides for alternate delivery of charge packets at the output amplifiers.

A Gated Charge Detector/Amplifier — Charge packets are transported to a precharged capacitor whose potential changes inearly in response to the quantity of the signal charge delivered. This potential is applied to the input gate of the two-stage NMOS amplifiers producing a signal at the output "V_{OUT}" pin Before each charge packet is sensed, a reset clock (ϕRA, ϕRB) recharges the input node capacitor to a fixed voltage (V_{RDA}, V_{RDB})

Integration and Anti-Blooming Controls — In many applications the dynamic range in parts of the image is larger than the dynamic range of the CCD, which may cause more electrons to be generated in the photosite area than can be stored in the CCD shift register. This is particularly common in industrial inspection and satellite applications. The excess electrons generated by bright illumination tend to "bloom" or "spill over" to neighboring pixels along the shift register, thus "smearing" the information. This smearing can be eliminated using two methods:

Anti-Blooming Operation:

A DC voltage applied to the integration control gate (approximately 5 to 7 volts) will cause excess charge generated in the photosites to be diverted to the anti-blooming sink (V_{SINK}) instead of to the shift registers. This acts as a "clipping circuit" for the CCD output (see Fig. 2). See also page 238 for further details

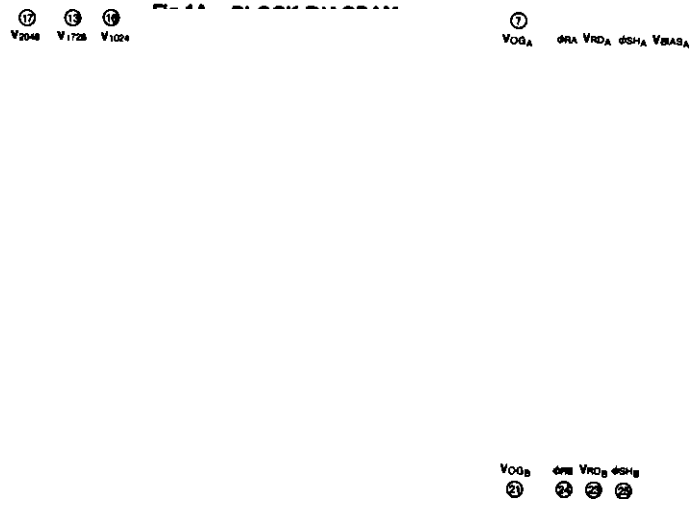


Fig. 1B CIRCUIT DIAGRAM NEAR PIXEL #1024

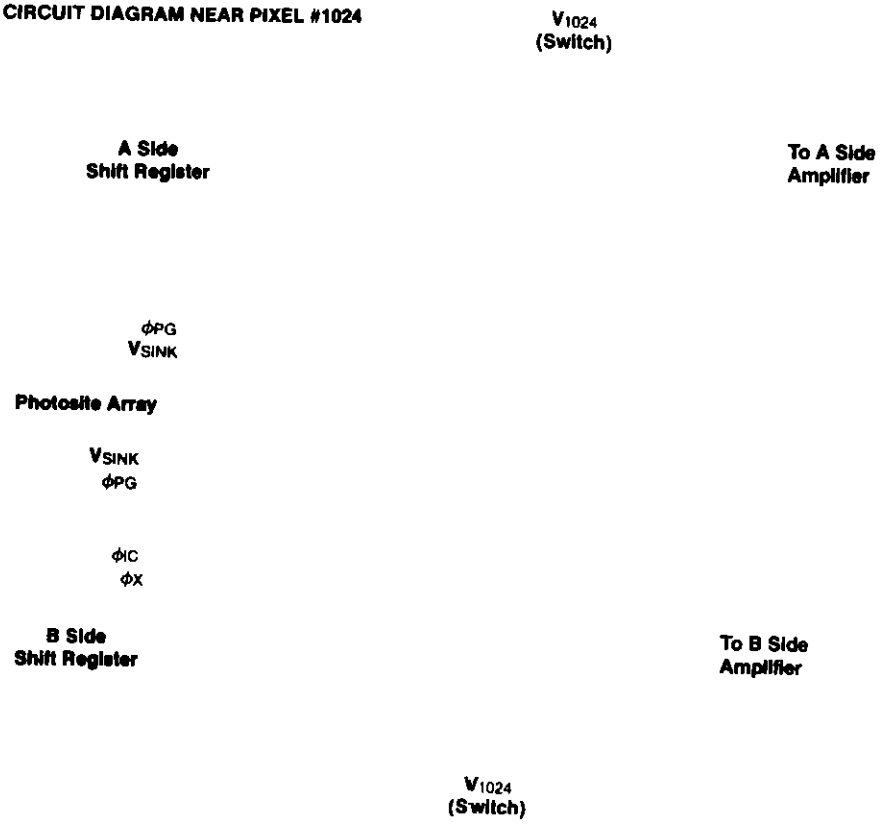


Fig. 2 MAXIMUM OUTPUT VOLTAGE vs. ϕ_{IC} Voltage

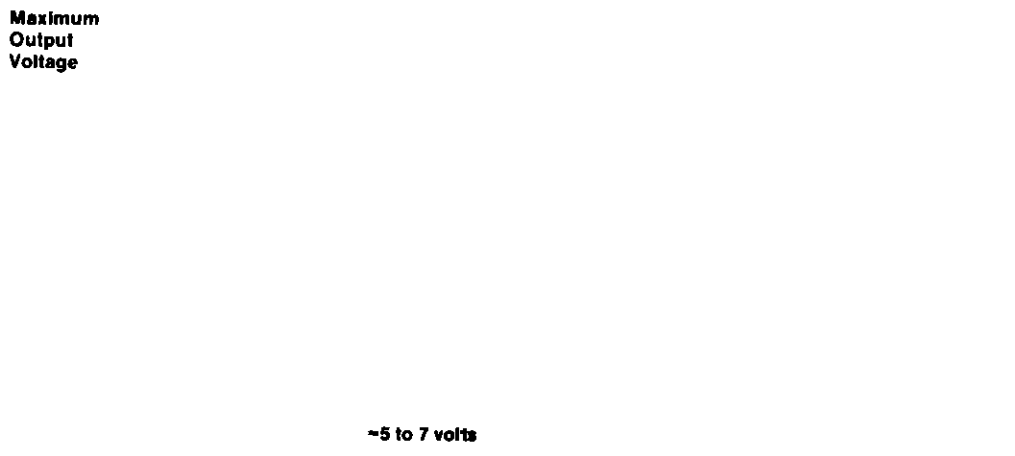


Fig. 3 INTEGRATION-CONTROL TIMING DIAGRAM

1 t1 > t_{fall} of ϕX.

(Note 4)

o the shift registers during ϕx clock-high period. Photosite charge > Q_{SAT} ized.

r V_{SS}(−2V).
0.0 to 0 7 volts and ϕ_{IC} clock-high = same range as ϕ_1 clock-high

Integration Control Operation:
Variable integration times which are less than the CCD

The integration-control and anti-blooming features can be implemented simultaneously. This is done by setting the ϕ_{IC} clock-low level to approximately 5 to 7 volts. (See application note on page 238 for further discussion).

DEFINITION OF TERMS

Charge-Coupled Device — A charge-coupled device is a semiconductor device in which finite isolated charge packets are transported from one position in the semiconductor to an adjacent position by sequential clocking of an array of gates. The charge packets are minority carriers with respect to the semiconductor substrate.

Sample-and-Hold Clock (ϕ_{SHA}, ϕ_{SHB}) — The voltage waveform applied to the sample-and-hold gates in the output amplifiers to create a continuous sampled video signal at the output. The sample-and-hold feature may be defeated by connecting ϕ_{SHA} and ϕ_{SHB} to V_{DD}.

Dark Reference — Video output level generated from sensing elements covered with opaque metalization which provides a reference voltage equivalent to device operation in the dark. This permits use of external DC restoration circuitry.

Isolation Cell — This is a site on-chip producing an element in the video output that serves as a buffer between valid video data and dark reference signals. The output from an isolation cell contains no valid information and should be ignored.

Dynamic Range — The saturation exposure divided by the RMS temporal noise equivalent exposure. Dynamic range is sometimes defined in terms of peak-to-peak noise. To compare the two definitions a factor of four to six is generally appropriate in that peak-to-peak noise is approximately equal to four to six times RMS noise.

RMS Noise Equivalent Exposure — The exposure level that gives an output signal equal to the RMS noise level at the output in the dark.

Saturation Exposure — The minimum exposure level that will provide a saturation output signal. Exposure is equal to the light intensity times the photosite integration time.

Charge Transfer Efficiency — Percentage of valid charge information that is transferred between each successive stage of the transport registers.

Responsivity — The output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure.

Total Photoresponse Non-Uniformity — The difference of the response levels of the most and the least sensitive element under uniform illumination. Measurement of PRNU excludes first and last elements.

Dark Signal — The output signal in the dark caused by thermally generated electrons that is a linear function of the integration time and is highly sensitive to temperature.

Saturation Output Voltage — The maximum useable signal output voltage. Charge transfer efficiency decreases sharply when the saturation output voltage is exceeded.

Integration Time — The time interval between the falling edge of the integration clock and the falling edge of the transfer clock. The integration time in which charge is accumulated in the photosites.

Exposure Time — The time interval between the falling edge of the two transfer pulses (ϕX) as shown in the timing diagram. The exposure time is the time between transfers of signal charge from the photosites into the transport registers.

Pixel — A picture element (photosite).

Fig. 4: PHOTOELEMENT DIMENSIONS

TEST LOAD CONFIGURATION

ABSOLUTE which useful life

Storage Temperature	-25° C to +125° C
Operating Temperature	-25° C to +70° C
CCD 181: Pins 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 27	-0.3V to +18V
Pin 1	0V
Pins 14, 15, 28	-3.0V to 0V
Pins 2, 26	See Caution Note

CAUTION NOTE:
These devices have limited built-in gate protection. It is recommended that static discharge be controlled and minimized. Care must be taken to avoid shorting pins $V_{OUT_{A+B}}$ to V_{SS} or V_{DD} during operation of the devices. Shorting these pins temporarily to V_{SS} or V_{DD} may destroy the output amplifiers.

DC CHARACTERISTICS: $T_P = 25°C$ (Note 1)

SYMBOL	CHARACTERISTIC	RANGE MIN	RANGE TYP	RANGE MAX	UNIT	CONDITION
V_{DD}	Output Amplifier Drain Supply Voltage	13.5	14.0	14.5	V	
$V_{RD\ (A+B)}$	Output Reset Drain Supply Voltages	13.5	14.0	14.5	V	
V_{SINK}	Anti-Blooming Sink Voltage	13.5	14.0	14.5	V	
V_{PG}	Photogate Bias Voltage	5.5	6.0	6.5	V	
$V_{OG\ (A+B)}$	Output Gate Bias Voltages	5.5	6.0	6.5	V	
$V_{BIAS\ (A+B)}$	Amplifier Bias Voltages	2.5	3.0	3.5	V	
V_{SG}	Amplifier Signal Ground	0.0	0.3	0.5	V	
V_{SS}	Substrate Ground	-3.0	-2.0	-1.0	V	Note 2
I_{DD}	Output Amplifier Drain Supply Current	6.0	10.0	15.0	mA	

CLOCK CHARACTERISTICS: $T_P = 25°C$ (Note 1)

SYMBOL	CHARACTERISTIC	RANGE MIN	RANGE TYP	RANGE MAX	UNIT	CONDITIONS
$V\phi X$ HIGH	Transfer Clock HIGH	11.0	11.5	12.0	V	Note 3
$V\phi 1$ HIGH (A+B) $V\phi 2$ HIGH (A+B)	Transport Clock HIGH	9.5	10.0	10.5	V	Note 3
$V\phi R$ HIGH (A+B)	Reset Clock HIGH	11.0	11.5	12.0	V	Note 3
$V\phi SH$ HIGH (A+B)	Sample/Hold Clock HIGH	11.0	11.5	12.0	V	Note 3
$V\phi 1024$ HIGH	Select 1024 Elements Clock HIGH	9.5	10.0	10.5	V	Note 3
$V\phi 1728$ HIGH	Select 1728 Elements Clock HIGH	9.5	10.0	10.5	V	Note 3
$V\phi 2048$ HIGH	Select 2048 Elements Clock HIGH	9.5	10.0	10.5	V	Note 3
$V\phi IC$ HIGH	Integration Control Clock HIGH		10.0		V	Note 3
$V\phi IC$ LOW	Integration Control Clock LOW		6.0		V	Note 2, 3
$V\phi X$ LOW	Transfer Clock LOW	0.0	0.3	0.7	V	Note 2, 3
$V\phi 1$ LOW (A+B)	Transport Clock LOW	0.0	0.3	0.7	V	Note 2, 3
$V\phi 2$ LOW (A+B)	Transport Clock LOW	0.0	0.3	0.7	V	Note 2, 3
$V\phi R$ LOW (A+B)	Reset Clock LOW	0.0	0.3	0.7	V	Note 2, 3
$V\phi SH$ LOW (A+B)	Sample/Hold Clock LOW	0.0	0.3	0.7	V	Note 2, 3
$V\phi 1024$ LOW	Select 1024 Elements Clock LOW	0.0	0.3	0.7	V	Note 2, 3, 5
$V\phi 1728$ LOW	Select 1728 Elements Clock LOW	0.0	0.3	0.7	V	Note 2, 3, 5
$V\phi 2048$ LOW	Select 2048 Elements Clock LOW	0.0	0.3	0.7	V	Note 2, 3, 5
f_{data} max	Maximum Output Data Rate	10.0	20.0		MHz	Note 6

AC CHARACTERTISTICS: $T_P = 25°C$, (Note 1, 7), $f_{data} = 3.0MHz$, $t_{int} = 10ms$, Light Source=2854°K + 2.0mm thick Schott BG-38 and OCLI WBHM Filters (Note 4). All tests done using "Test Load Configuration."

SYMBOL	CHARACTERISTIC	RANGE MIN	RANGE TYP	RANGE MAX	UNIT	CONDITIONS
DR	Dynamic Range (relative to peak-to-peak noise) (relative to rms noise)		1500:1 7500:1			
NEE	RMS Noise Equivalent Exposure		50×10^{-6}		$\mu J/cm^2$	
SE	Saturation Exposure		0.3		$\mu J/cm^2$	
CTE	Charge Transfer Efficiency	.99996	.99999			Note 8
Vo	Output DC Level	4.0	9.5	11	V	
Z	Output Impedance		1		K Ω	
P	On-Chip Power Dissipation: Amplifiers		159	200	mW	
N	Peak-to-Peak Temporal Noise		0.7		mV	

PERFORMANCE CHARACTERISTICS: T_P = 25°C (Note 1, 7), f_{data} = 3.0MHz, t_{int} = 1.0ms, Light Source = 2854°K + 2.0mm thick Schott BG-38 and OCLI WBHM filters (Note 4).

	MIN		MAX	UNIT	CONDITION
Photoresponse Non-uniformity					
Peak-to-Peak		55	120	mV	
Peak-to-Peak without single pixel and Positive and Negative Pulses		35		mV	
Single-pixel Positive Pulses		30		mV	
Single-pixel Negative Pulses		30		mV	
Video Mismatch		50	150	mV	Note 9
DC Mismatch		0.5	2.0	V	Note 10
Dark Signal:					Notes 11, 12
DC Component		1	2	mV	
Low Frequency Component		1	2	mV	
Single Pixel DS Non-Uniformity		1	2	mV	Note 12
Responsivity		4.0		V/μJ/cm^2	
Saturation Output Voltage	0.7	1.0	2.0	V	

* All PRNU measurements are taken at an 800 mvolt output level using an f/5.0 lens and exclude the output from the first and last elements of the array. The "f" number is defined as the distance from the lens to the array divided by the diameter of the lens aperature. As the "f" number increases, the resulting more highly collimated light causes the package window imperfections to dominate and increase PRNU. A lower "f" number results in less collimated light causing device photosite blemishes to dominate the PRNU.

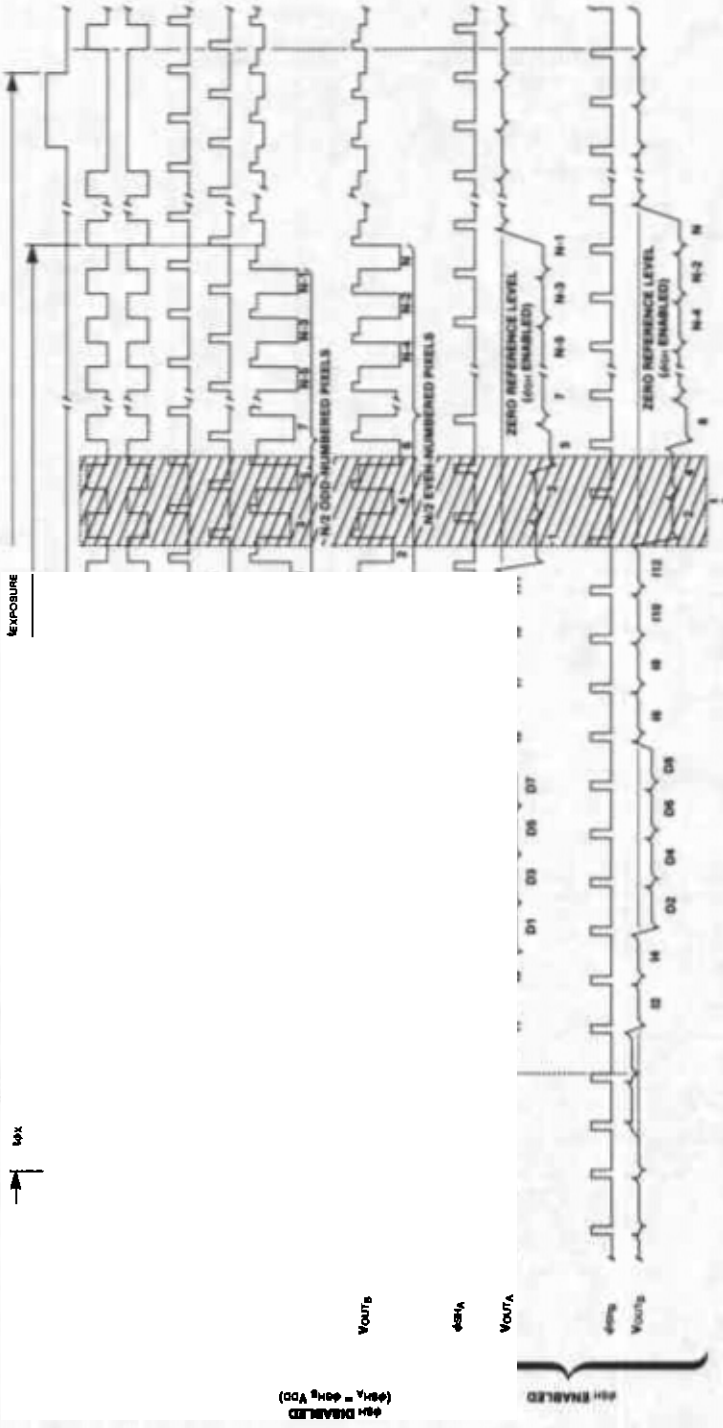
NOTES:

1. T_P is defined as the package temperature measured on a copper block in good thermal contact with the entire backside of the package.
2. Negative transients on any clock pin going below 0.0 volts may cause charge injection, which results in an increase in apparent DS. Adjusting V_{SS} to a more negative voltage than the clock low voltages will reduce charge injection, if present.
3. $C\phi_X$ = 150pF, $C\phi_{EC}$ = 250pF, $C\phi_{1A} = C\phi_{1B} = C\phi_{2A} = C\phi_{2B}$ = 300pF
   $C\phi_{RA} = C\phi_{RB} = C\phi_{SHA} = C\phi_{SHB}$ = 5pF, $V_{1024} = V_{1728} = V_{2048}$ = 5pF
4. OCLI WBHM = Optical Coating Laboratory, Inc. Wide Band Hot Mirror.
5. Pixel Length Selection
   (a) To use the device with 2592 active pixel elements.
   Connect V_{1024}, V_{1728}, and V_{2048} to the ϕ_2 (A or B) clock
   (b) To use the device with 2048 active pixel elements:
   Connect V_{1024}, V_{1728} to the ϕ_2 (A or B) clock.
   Connect V_{2048} to V_{SS}
   (c) To use the device with 1728 active pixel elements:
   Connect V_{1024} and V_{2048} to the ϕ_2 (A or B) clock
   Connect V_{1728} to V_{SS}
   (d) To use the device with 1024 active pixel elements:
   Connect V_{1728} and V_{2048} to the ϕ_2 (A or B) clock
   Connect V_{1024} to V_{SS}

ıUT A and V_{OUT} B under uniform illumination. it can be eliminated by

and V_{OUT} B
n T_P
of the SPDSNU. The SPDSNU approximatley doubles for every 5 to 15°C

CCD181 TIMING DIAGRAM



NPUTS TO $V_{SW\ TCH}$ P NS

N
1024
1728
2048
2592

V_{SS} ϕ_2

V_{switch} pins and the $\phi 2_A$ and $\phi 2_B$ pins

) has been omitted from these timing
ration Control Clock Timing" diagram

ϕ_{SH} DISABLED
($\phi SH_A = \phi SH_B\ V_{DD}$)

ϕ_{SH} ENABLED

$\phi 2_A = \phi 2_B$

$\phi 1_A = \phi 1_B$

ϕR_A

ϕR_B

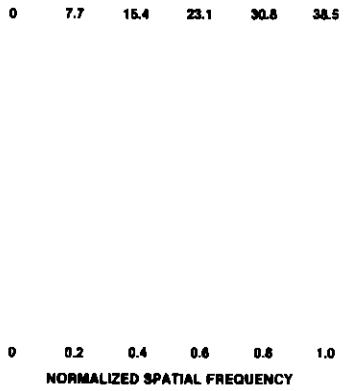
V_{OUT_A}

V_{OUT_B}

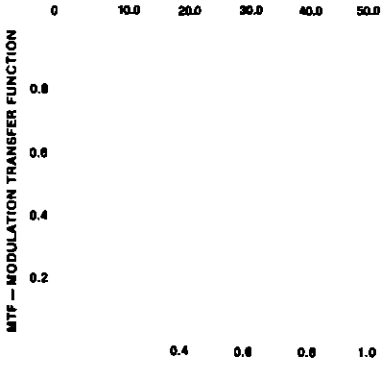
VALID VIDEO
PIXEL #2

TYPICAL PERFORMANCE CURVES

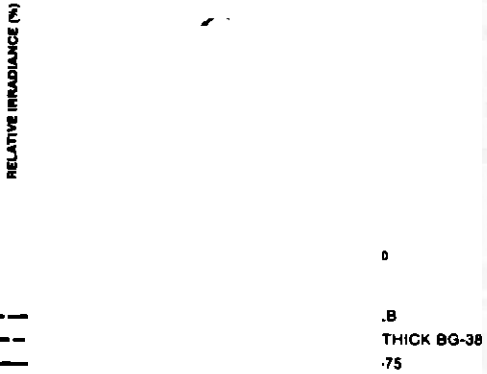
MODULATION TRANSFER FUNCTIONS FOR TWO BROADBAND ILLUMINATION SOURCES



MODULATION TRANSFER FUNCTIONS FOR NARROW BAND ILLUMINATION SOURCES

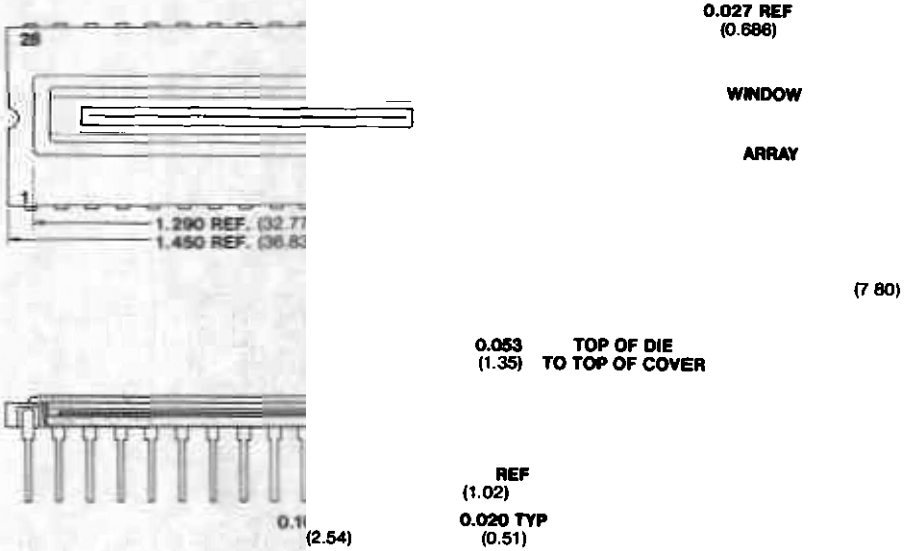


SINGLE-PIXEL DARK SIGNAL NON-UNIFORMITIES VERSUS INTEGRATION TIME



DC AND LOW-FREQUENCY DARK SIGNAL VS INTEGRATION TIME

PACKAGE OUTLINE
28-Pin Dual In-line Ceramic Package



NOTES

All dimensions in inches (bold) and millimeters (parentheses) Header is black ceramic (Al_2O_3). Window is glass. The amplifier of the device is located near the notched end of the package

DEVICE CARE AND OPERATION

Glass may be cleaned by saturating a c
and lightly wiping the surface. Rinse
de-ionized water. Allow the glass to dry
with filtered dry N_2 or air.

It is important to note in design and ap
tions that the devices are very sensitive
The dark signal DC and low frequency
mately double for every 5° C temperatu
pixel dark signal non-uniformities app
every 12° C temperature increase. The
to achieve very long integration times
capability.

ORDER INFORMATION

Order CCD181DC where "D" stands for a ceramic package and "C" for commercial temperature range.

Area Scan CCD Sensors

The CCD222 Series Area Scan Sensor are very high performance devices intended for use in broadcast quality camera systems and in the most demanding industrial and scientific applications

FAIRCHILD WESTON

CCD IMAGING DIVISION

CCD 222
488×380-Element Area Image Sensor

FEATURES

- 185,440 sensing elements on a single chip
- Available horizontal resolution: 380 elements per line
- Available vertical resolution: 488 lines
- No lag, no geometric distortion
- A gamma of unity
- High dynamic range — typically > 1,000:1 at 25°C (excluding dark signal non-uniformity)
- Low light level capability, low noise equivalent exposure
- Video data rates up to 20 MHz, frame rates to 90 Hz
- Sample-and-hold video output
- Low power dissipation, solid-state reliability and small size
- Standard TV aspect ratio (4:3)
- Satisfies NTSC resolution standards
- Two-phase register clocking
- Digitally-controlled readout
- Special selections available — consult factory.

DESCRIPTION

The low noise performance of the buried channel CCD structure provides excellent low-light-level capabilities when the sensor is cooled; performance adequate for most applications can be achieved with the sensor at

CCD222 488X380 Element Area Image Sensors are also included in Fairchild Weston's series of solid-state television camera systems.

PIN NAMES

AB	Anti-Blooming Bias (for Column Anti-Blooming)
SF	Floating-Gate Amplifier Source Bias
$VIDEO_{OUT}$	Amplifier Output
ϕ_P	Photogate Clock
ϕ_{V1}, ϕ_{V2}	Vertical Transport Clocks
ϕ_{H1}, ϕ_{H2}	Horizontal Transport Clocks
ϕ_{BE}	Bias Electrode Clock
ϕ_R	Reset Clock
ϕ_S	Sample-and-Hold Clock
V_{RD}	Reset Bias
V_{DD}	Output Amplifier Drain Supply
V_{SS}	Substrate (GND)
TP	Test Points

CCD222 CONNECTION DIAGRAM (TOP VIEW)

* PIN 1 (V_{SS}) IS DESIGNATED BY A DOT ON SIDE OF PACKAGE.

Fairchild Weston Systems, Inc. CCD Imaging Division.
610 W. Maude Ave., Sunnyvale, California 94086
408-720-7600, TWX 910-373-2110

CCD222 BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION

The CCD222 consists of the functional elements illustrated in the Block Diagram:

Image Sensing Elements

Image photons pass through a transparent polycrystalline silicon gate structure and are absorbed in the silicon crystal structure creating hole-electron pairs. The resulting photoelectrons are collected in the photosites during the integration period. The amount of charge accumulated in each photosite is a linear function of the localized incident illumination intensity and the integration period.

Vertical Transport Registers

The interline transfer architecture of the CCD222 provides video information in two sequential fields of 244 lines each. At the end of an integration period, when the photogate voltage ϕ_P is lowered and the ϕ_{V1} clock is HIGH, charge packets from odd-numbered photosite rows (1,3,5 . . . 487) are transferred to the vertical transport registers to initiate an odd-field readout. Clocking ϕ_{V1} and ϕ_{V2} transports the charge packets up the vertical transport registers where they are transferred line by line into the horizontal output register. After readout of the odd field, the ϕ_P voltage is again lowered and the ϕ_{V2} clock is HIGH causing transfer of charge packets from even numbered photosite rows (2,4,6. . . 488) into the vertical registers, thereby initiating an even-field readout.

Horizontal Analog Transport Register

The horizontal transport register is a 385-element 2-phase register that receives the charge packets from the vertical registers line by line. After each line of information is transferred from the vertical transport registers, it is moved serially to the output amplifier by the complementary horizontal clocks ϕ_{H1} and ϕ_{H2}. A minimum of 385 horizontal clock pulses are required to complete transfer of one line of information past the floating-gate amplifier.

Resettable Floating-Gate Amplifier

The charge packets from the horizontal transport register are sensed by a floating-gate whose potential changes linearly with the quantity of signal charge. The floating-gate is designed to be reset to the reset drain voltage V_{RD} by the reset clock, ϕ_R, after the completion of each horizontal line readout.

The output signal from the floating-gate drives a voltage amplification stage, is sampled and held under control of the sample clock ϕ_S by a sampling transistor switch and is buffered to the output terminal $VIDEO_{OUT}$ through a larger MOS transistor. The resultant video output signal is a sampled-and-held clock-controlled analog signal representing the spatial distribution of the exposure level at the sensor surface.

Sampled Video Output (See Timing Diagram)

The output waveform of the CCD222 is shown in detail in the Timing Diagram. Each frame (488 horizontal lines) is delivered to the output in two sequential fields of 244 horizontal lines each. Each horizontal line is 380 elements long and is preceded by 4 pre-scan elements which contain no video information, but are representative of the dark current levels in the horizontal register.

DEFINITIONS OF TERMS

Photogate Clock ϕ_P — The voltage waveform applied to the photogate.

Vertical Transport Clocks ϕ_{V1}, ϕ_{V2} — The clock signals applied to the vertical transport registers.

Horizontal Transport Clocks ϕ_{H1}, ϕ_{H2} — The clock signals applied to the horizontal transport register.

Resettable Floating-Gate Amplifier — The on-chip pre-amplifier which develops a signal voltage linearly proportional to the number of electrons contained in each sensed charge packet. The floating gate is coupled to the charge transport channel exclusively by electrostatic fields for low-noise signal detection.

Reset Clock ϕ_R — The clock applied to the gate of the reset switch to reset the voltage on the floating gate.

Sample-and-Hold Clock ϕ_S — The clock applied to the sample-and-hold gate of the amplifier. (The sample-and-hold feature can be disabled by connecting ϕ_S to V_{DD}).

Dynamic Range — The ratio of the saturation output voltage to the rms noise in the dark. The peak-to-peak random noise output of the device is 4-6 times the rms noise output.

Saturation Exposure — The minimum exposure level that will produce a saturated output signal. Exposure is equal to the product of light intensity and the integration time.

Spectral Response Range — The spectral band over which the response per unit of radiant power is more than 10% of the peak response.

Responsivity — The output signal voltage per unit exposure.

Photoresponse Shading Non-Uniformity — The differenc of the response levels between the most and the least sensitive regions under uniform illumination (excluding blemished elements) expressed as a percentage of the average response. Shading is measured using the digital equivalent of a low-pass filter with a cut-off frequency of approximately 5 cycles per picture width or picture height in the video output line.

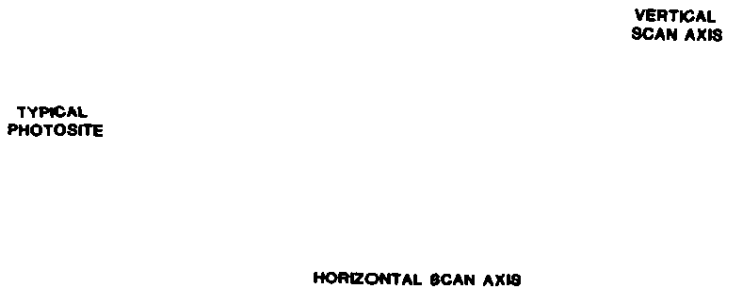
Dark Signal — The output signal in the dark caused by thermally generated electrons. Dark signal is a linear function of integration time and an exponential function of chip temperature.

Saturation Output Voltage — The maximum useful output signal amplitude.

Integration Time — In this device, the integration time is equal to the frame period when used in the standard mode of operation.

Pixel — Picture element or sensor element — also called photoelement or photosite.

PHOTOSITE DIMENSIONS



ABSOLUTE MAXIMUM RATINGS:

STORAGE TEMPERATURE	−100°C to +100°C
VOLTAGES:	
Pins 3, 4, 5, 6, 7, 20	−0.3V to +16V
Pins 2, 8, 9, 10, 11, 12, 13, 14, 17, 18, 19, 21, 22	−10V to +15V
Pin 1	V_{SS} = 0V
Pins 15, 16	NC

Caution Note

The devices do not have built-in gate protection It is crucial that static discharge be controlled and minimized. Care must be taken to avoid shorting pin $VIDEO_{OUT}$ to V_{SS} or V_{DD} during operation of the device

Dirty glass windows on devices cause increased photoresponse non-uniformity. Glass may be cleaned by saturating a cotton swab in alcohol and lightly wiping the surface Rinse off the alcohol with de-ionized water Allow the glass to dry, preferably by blowing with filtered dry N_2 or air

DC OPERATING CONDITIONS AND CHARACTERISTICS: Devices are tested at nominal conditions except for V_{SF}, which is adjusted for individual sensors.

		Range				
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Remarks**
V_{DD}	DC Supply Voltage	12.0	15.0	16.0	V	
V_{AB}	Anti-Blooming Bias Voltage		12.0		V	
V_{SF}	Source of Floating-Gate Amplifier	4.0	7.0	10.0	V	Note 1
V_{RD}	Reset Drain Voltage		4.0		V	
TP_1	Test Point		V_{DD}		V	
TP_2	Test Points		0.0		V	
TP_3, TP_4	Test Point	1.0	15.0	16.0		Note 10
I_{DD}	DC Supply (V_{DD}) Current				mA	
I_{SF}	Current at Pin SF		50		μA	

CLOCK CONDITIONS: Devices are tested at clock conditions which result in optimized performance in Fairchild equipment. Clock voltages are within ranges shown.

		Range				
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Remarks**
$V_{\phi PL}$	Photogate Clock LOW	−6.0	0.0		V	Note 2, 9
$V_{\phi PH}$	Photogate Clock HIGH	3.0	5.0	7.0	V	Note 2
$V_{\phi BEL}$	Bias Electrode of FGA Clock LOW	−3.0	0.0	0.0	V	
$V_{\phi BEH}$	Bias Electrode of FGA Clock HIGH	0.0	5.0	7.0	V	Note 1
$V_{\phi H1L}$ $V_{\phi H2L}$	Horizontal Transport Clock LOW	−5.0	0.0	0.0	V	Note 3
$V_{\phi H1H}$ $V_{\phi H2H}$	Horizontal Transport Clock HIGH	5.0	10.0	12.0	V	Note 1, 3
$V_{\phi V1L}$ $V_{\phi V2L}$	Vertical Transport Clock LOW	−6.0	0.0	0.0	V	Note 2, 9
$V_{\phi V1H}$ $V_{\phi V2H}$	Vertical Transport Clock HIGH	5.0	7.0	12.0	V	Note 4
$V_{\phi SL}$	Sample-and Hold Clock LOW	−3.0	0.0	0.0	V	
$V_{\phi SH}$	Sample-and-Hold Clock HIGH	3.0	5.0	7.0	V	
$V_{\phi RL}$	Reset Clock LOW	−6.0	0.0	0.0	V	
$V_{\phi RH}$	Reset Clock HIGH	5.0	7.0	12.0	V	
$f_{\phi H1}$ $f_{\phi H2}$	Horizontal Transport Clock Frequency		7.2	20.0	MHz	Note 5

PERFORMANCE SPECIFICATIONS: Standard test conditions are TV format data output at a 30 Hz frame rate, 60 Hz field rate, 15.75 kHz line rate, 7.16 MHz pixel rate, $T_c = 25°C$. Light source is 2854°K incandescent with 2.0 mm thick Schott BG-38 IR reject filter.

V_{SAT}	Saturation Output Voltage	700	mV_{P-P}	Note 6
DR	Dynamic Range	1000		See Definitions of Terms
SI	Saturation Irradiance	8.4	$\mu W/cm^2$	See Table A
R	Responsivity	0.08	$V/\mu W cm^{-2}$	
V_0	Output DC Level	7	V	3KΩ load resistance
P	Amplifier Power Dissipation		mW	3KΩ load resistance
Z	Output Impedance	1000	ohm	
CTF_H	Contrast Transfer Function, Horizontal	75	%	At 380 columns/ picture width
CTF_V	Contrast Transfer Function, Vertical	70	%	At 488 lines/ picture height
DSSNU	Dark Signal Shading Non-Uniformity	1	% V_{SAT}	See Definitions of Terms Note 7,8
PRSNU	Photo Response Shading	1	% V_{OUT}	See Definitions of Terms Note 7

NOTES

on.

ITSC rate of 30 frames per second. Higher clock rates are possible. Operation e. Two factors contribute to the fundamental low frequency limit: dark current formities, and dark current contributions in the register which will result in time, the higher the spatial non-uniformities.

ls and outer edge elements on a line or field basis.
(C) increase in chip temperature.
evel of these clock signals is between 0 and -6V with respect to V_{SS}.
upply. On devices date coded 86-52 or earlier, connect TP_3 to 0.0V.

TABLE A

TYPICAL SATURATION IRRADIANCE LEVELS OF CCD222 AT 30 FRAMES/SEC.

Photometric[d]

a. 1 $\mu W/cm^2 = 0.22$ lux
b. 1 $\mu W/cm^2 = 1.5$ lux. The 900nm cutoff filter blocks wavelengths above approximately 900nm. Use a Corning 1-75 glass filter 3mm thick.
c. 1 $\mu W/cm^2 = 3.0$ lux. The 700nm cutoff filter blocks wavelengths above approximately 700nm. Use a Schott BG-38 glass filter 2mm thick.
d. 1 fc = 10.76 lux.

COSMETIC PERFORMANCE SPECIFICATIONS

The CCD222 is a very high performance device intended for use in broadcast quality camera systems and in the most demanding industrial and scientific applications. A CCD222 element is considered to be blemished if it exhibits a spurious output (in comparison to its nearest neighbors) of more than 10% of V_{SAT}. Blemish content is determined in the dark, and at an illumination level of 50% V_{SAT}. Single-point Blemishes (SPB's) are sometimes found in CCD222 sensors; horizontal line and column oriented defects are rarely found because of Fairchild's choice of device structure.

Devices exhibiting less stringent performance and/or cosmetic specifications may be obtainable by negotiation.

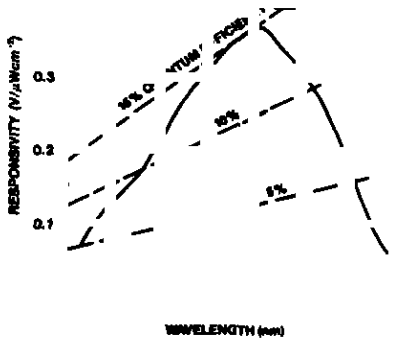
BLEMISH SPECIFICATIONS FOR CCD222:

(Measured at $T_A = 25°C$ and at uniform light levels developing 0, 25 and 50% of V_{SAT}.)

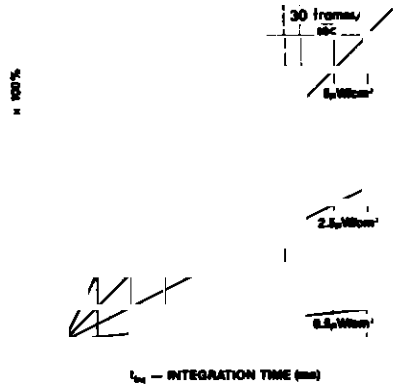
Characteristic	CCD222A Max
Number of Single Point Blemishes	5
Largest SPB Dimension	2
Number of Blemished Pixels in SPB's	10
Number of Column Defects	0
Widest Column Defect Width	0
Number of Defective Columns	0

TYPICAL PERFORMANCE CURVES

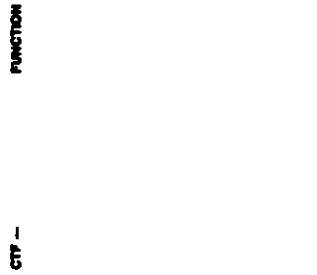
TYPICAL SPECTRAL RESPONSE



OUTPUT SIGNAL LEVEL VERSUS INTEGRATION TIME 2854°K TUNGSTEN SOURCE WITH SCHOTT BG-38 FILTERS



HORIZONTAL CONTRAST TRANSFER FUNCTION FOR TWO BROADBAND ILLUMINATION SOURCES



VERTICAL CONTRAST TRANSFER FUNCTION FOR TWO BROADBAND ILLUMINATION SOURCES

FIGURE 1:

16.6ms ODD FIELD

EVEN FIELD

ØP

ØV1=ØR

ØV2

ØH1=ØBE

ØH2

ØS

VIDEO$_{out}$

FIGURE

FIGURE 3

ØP

ØV1=ØR

ØV2

ØH1=ØBE

ØH2

ØS

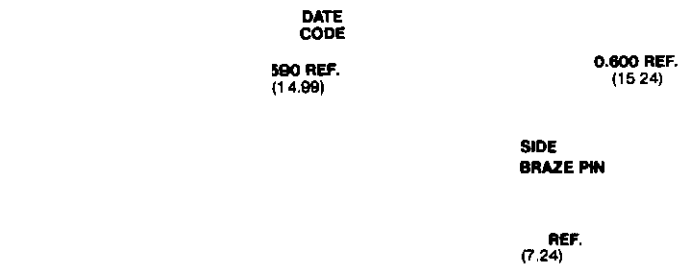
here correspond to this

required. They may be

OUTPUT WAVEFORM ($VIDEO_{OUT}$) UNDER UNIFORM ILLUMINATION (= 50% V_{SAT})

CCD222 PACKAGE OUTLINE

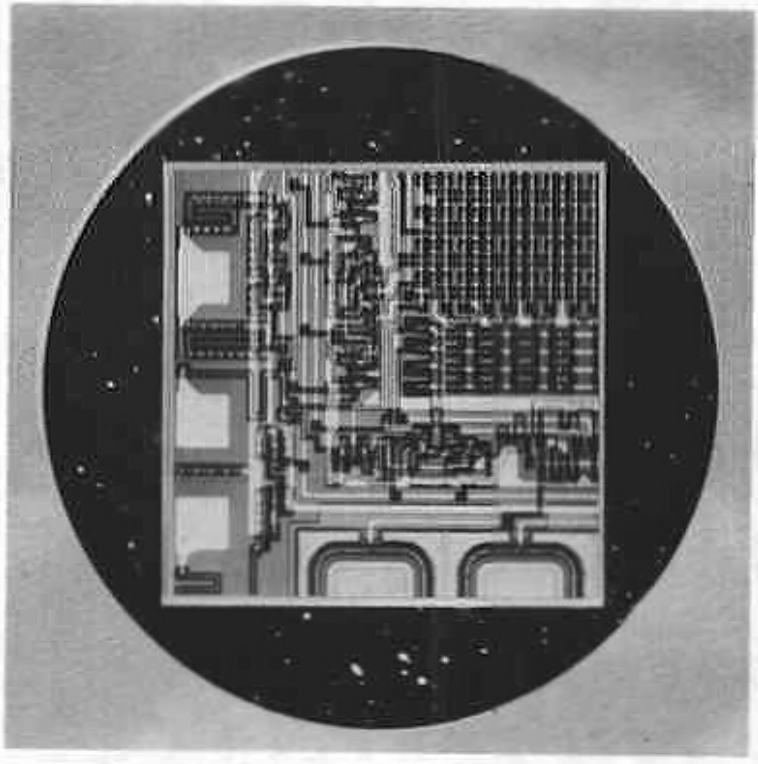
22-Pin Ceramic Package



(1.52) NOTES: All dimensions in inches (bold) and millimeters (parentheses). Header is black ceramic (Al_2O_3). Glass window is attached to header with epoxy cement

ORDER INFORMATION

Description	Device Type Order Code
CCD222(Class A Blemish Spec.)	CCD222ADC



CCD Design Development Aids

Fairchild Weston offers printed circuit boards to assist customers in initial experiments with CCD devices. All design development boards do include the sensor and require customer development of optical inputs and processing of the CCD output signal.

FAIRCHILD WESTON

CCD IMAGING DIVISION

I-SCAN
Design Development Board
CCD111 Sensor

I-SCAN consists of a Fairchild CCD111, 256 element line scan sensor, mounted on a printed circuit card that contains all the necessary CCD111 operating electronics. It is intended for use as a construction aid for experimental systems using CCD line scan sensors or can be incorporated directly into systems requiring 256 elements of resolution. I-SCAN comes fully assembled and tested and requires only the input of power supplies and an oscilloscope to display the video information corresponding to the image placed in front of the sensor.

The I-SCAN card, Figure 1, measures 4½ by 4 inches. The CCD111 is mounted in a socket centrally located on the card. A lens maybe positioned in front of the sensor to focus an image onto the array. All board I/O connections are made through a 22 position single edge card connector with .156 inch center-pacings. The edge connector is compatible with TRW/CINCH type 50-44A-30 or equivalent.

The board circuit, Figure 2, requires a power supply input of +15V at 100mA to Pin 1 and +5V at 200mA to Pin 4. The ground returns should go to Pin 22.

An on-board regulator provides a clock high level voltage of 8V. The +15V supply is divided to achieve a 12V reset drain voltage and a 10V photogate bias voltage required by the CCD111. The output gate voltage, V_{OG} is derived from the +5V* supply.

For normal self-contained operation of the board, Pin 18, the internal/external master clock select line and Pin 12, the internal/external exposure time select are left open.

Voltage controlled oscillator U1 generates a master video clock signal which may be adjusted from approximately 1MHz to 4MHz by potentiometer R1. The frequency of the video clock square wave from U1 is divided by two by flip-flop U3A and one-half of MOS driver U7 amplifies the flip-flop output to provide the ϕR reset clock signal required by the CCD111. The normal amplitude of the ϕR clock signal at the sensor terminal is from a low of about 0.5V to a high of about 8V in accordance with the sensor data sheet recommendations.

The output from U3A is also fed into flip-flop U3B causing another divide by two used in generating the $\phi 1$ and $\phi 2$ transport clock signals. The outputs of U3B are fed into MOS driver U6 producing transport clock swings of from a low of about 0.5V to a high of 8.0V. Overall sensor data rate is equal to the ϕR clock frequency.

The exposure time of the sensor is controlled internally by one-shot U4B. Length of exposure time is adjusted with R6 giving times > 1mS. To begin an exposure, one shot U4B triggers one-shot U4A; a fast pulse from U4A resets counter U5 and starts it counting. The counting of U5 controls the ϕX transfer pulse through one-half of MOS driver U7. It also stops the transport clocks $\phi 1$ and $\phi 2$ during the transfer pulse internal in accordance with CCD111 data sheet recommendations. (See Figure 3.) Note that both transfer clocks ϕX_A and ϕX_B are tied together to achieve a satisfactory transfer.

F FRONT VIEW

PINS ON BACKSIDE

– – – DENOTES JUMPER WIRE

*Adjustment of V_{OG} over the range of 4-7V may be required for optimum operation of the sensor.

NOTICE

This Development Board may not present the optimum test conditions for your design [See application information on page 238].

Figure 2

After the transfer is completed, counter U5 restarts transport clocks $\phi 1$ and $\phi 2$, and disables itself until its next reset command at the start of the next exposure period.

Registors R9-R12 tie the open collector outputs of the MOS drivers to the clock high level voltage and clamp diodes CR3-CR6 tied to voltage V_{CL} prevent clock signal excursions below ground. Negative clock line transients at the CCD terminals can cause charge-injection which may result in an apparent increase in the dark signal non-uniformity of the sensor.

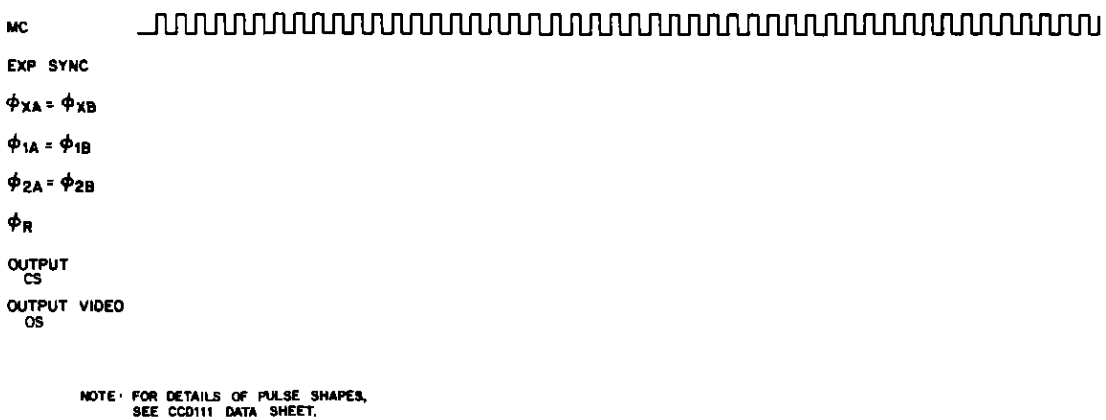
If Pin 18 of the card is held low, an external master clock (TTL Level) may be input on Pin 19. Data rate of the sensor will equal one-half the frequency supplied to Pin 19. If Pin 12 is held low, the sensor will respond to an external (TTL Level) exposure signal on Pin 20. The exposure signal may be operated asynchronously with the data rate clock. Note in the timing diagram, however, that the $\phi 1$ transport clock signal is in the high state at the time of the exposure pulse.

In order not to mix two lines of video information in the transport registers of the CCD, the exposure or integration time of the sensor must be greater than the time necessary to read all the information from the previous line out of the transport registers. (i.e., $t_{INT} > \times 1$
(See Timing Diagram) F DATA CLOCK

Card connector fingers 14 and 15 provide exposure time sync and master clock output signals respectively for external usage; i.e., for synchronizing an oscilloscope for display of the sensor output signals.

The video output and compensation output of the CCD111 sensor are buffered through emitter followers and are made available on connector fingers 9 and 7 respectively. If long co-axial cables are wired to the outputs, the cables should be terminated into 75Ω for best frequency response. The cable terminations will reduce the video signal amplitudes by one-half

Figure 3 **I-SCAN TIMING DIAGRAM**



NOTE: FOR DETAILS OF PULSE SHAPES, SEE CCD111 DATA SHEET.

FAIRCHILD WESTON

CCD IMAGING DIVISION

CCD122DB
Design Development Board
CCD122 Sensor

The Fairchild CCD122DB Design Development Board is a printed circuit card which is intended for use as an educational

The board measures 4½ by 5 inches. A socket for installation of the charge coupled device line scan sensor is mounted centrally on the back (wiring) side of the card. The user can position a lens in front of the sensor if required for his study. Board I/O connections are made through a 22 position double readout edge card connector with .156 inch center-to-center finger spacings. The edge connector is compatible with a TRW/CINCH type 50-44B-10 or equivalent.

The CCD122 should be inserted into the center of the socket so that socket terminals 1, 14, 15, and 28 are left open

The circuit board, requires a power supply input of 15+2V at 250mA maximum to Pins 1 and A of the edge card connector. The power supply return is wired to card edge fingers 22 and Z.

Three regulators on the design development boards provide a V_{DD} sensor supply voltage which is adjusted to +12.0V, a clock high level voltage which is set to +10.0V, and a +5V V_{CC} required by the TTL logic circuitry.

For normal self-contained operation of the board, Connector Terminals 3 and 5 are left open. Voltage Controlled Oscillator U1 generates a video clock signal which may be adjusted from approximately .5 to 2.0 MHz by potentiometer R1. VCO U1

recommendations. The ϕ_R reset clock signal is generated by U1 and flip-flop U2A and is amplified through U5 to deliver a ϕ_R clock frequency twice that of ϕ_T to the sensor.

One-shot U7A and JK flip-flop U3A and U3B develop a properly synchronized ϕ_X signal which is amplified by the second half of the 9644 driver U4. The interval between ϕ_X pulses is the exposure time for the sensor; exposure time may be adjusted by R2.

terminals can cause charge-injection which may result in an apparent increase in the dark signal non-unformity of the sensor.

Connector Figures 7 and 9 provide exposure time and data rate clock output signals for external usage; i.e., for synchronizing an oscilloscope for display of the sensor output signals.

The dc bias voltage applied to the V_T transport register electrodes and VEI bias voltage electrodes are preset to give optimal performance of the transport clock, white reference and end-of-scan signals. VEI may be increased to V_{DD} to disable the white reference level generating circuitry within the sensor.

The video output register signal (V_{OUT}) passes through a simple 2 MHz cutoff low pass filter formed by Q1, Q2 and associated capacitance and resistance circuits and is then routed off the board at connector finger 11 through 75 ohm resistor R24. Capacitors CX1, CX2 and CX3 may be installed by the user to provide high frequency rolloff as required to reduce high frequency on the output video signal.

The end-of-scan pulse (V_{EOS}) is buffered by Q3 and sent off the board at connector finger 13 through 75 ohm resistor R27. This pulse indicates that the readout of a line of video information is completed. The EOS pulse was injected into the EOS register by transfer pulse ϕ_X applied to the sensor U6 at pin 16

NOTICE

This Development Board may not present the optimum test conditions for your design [See application information on page 236].

NOTE

1.

2.

3.

4.

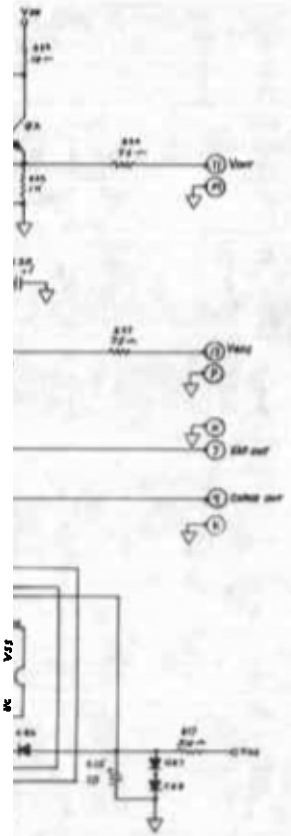
5.

6.

7.

8.

9.



LID II CCD 142/122

FAIRCHILD WESTON

CCD IMAGING DIVISION

CCD133DB/143DB/153DB Design Development Board CCD143A Sensor CCD133A Sensor CCD153A Sensor

The Fairchild Weston CCD133DB, CCD143DB and CCD153DB

The currently available CCD133DB/143DB/153DB Board does not utilize the following optional features of these devices:

- Improved Linearity by biasing V_{RD} at lower voltage than V_{DD}. (CCD133A, 143A, 153A).
- Non-sample-and-held output video waveform for external processing and/or further linearity improvements (CCD143A only).

The boards are 4½ by 5 inches. A socket for installation of the charge coupled device line scan sensor is mounted centrally on the back (wiring) side of the card. The user can readily mount a lens in front of the sensor if required for his study. Board I/O connections are made through a 44 position double readout edge card connector with .156 inch center-to-center finger spacings. The edge connector is compatible with a TRW/CINCH type 50-44B-10 or equivalent.

When a CCD143A is being used with a design development board, it should be installed in the sensor connector in normal fashion. When a CCD133A or a CCD153A is being used, it should be inserted into the center of the socket so that socket terminals 1, 14, 15, and 28 are left open.

The circuit board, requires a power supply positive input of +20±2V at 300mA maximum to Pins 1 and A of the edge card connector. Ground the power supply to pins 22 and Z of the edge card connector.

Three regulators on the design development boards provide a V_{DD} sensor supply voltage which is adjusted to +15.0V, a clock high level voltage which is set to +12.0V, and a +5V V_{CC} required by the TTL logic circuitry.

For normal self-contained operation of the board, Connector Terminal 17 is left open. Voltage Controlled Oscillator U1 generates a video clock signal which may be adjusted from approximately 5 to 20 MHz by potentiometer R1. The frequency of the video clock square wave from U1 is divided by two by flip-flop U2A; one-half of MOS driver U4 amplifies the flip-flop output to provide the ϕ_T transport clock signal required by the CCD image sensor. The normal amplitude of the ϕ_T clock signal at the sensor terminal is from a low of about 0.5V to a high of about 11.5V, in accordance with the sensor data sheet recommendations. Sensor characteristics at other clock conditions can be evaluated by adjustment of R28.

One-shot U7A and JK flip-flop U2B develop a properly synchronized ϕ_X signal which is amplified by the second half of the 9644 driver U4. The interval between ϕ_X pulses is the exposure time for the sensor; exposure time may be adjusted by R2.

In keeping with good high frequency engineering practice, damping resistors R6 and R7 are used in the MOS driver output lines to minimize overshoot and ringing contents in the clock signals supplied to the CCD. Clamp diodes CR3 and CR4 are used to prevent CCD clock signal excursions below ground; negative clock line transients at the CCD terminals can cause charge-injection which may result in an apparent increase in the dark signal non-uniformity of the sensor. R6 and R7 may need to be increased for operation of the CCD133A and CCD153A to prevent charge infection.

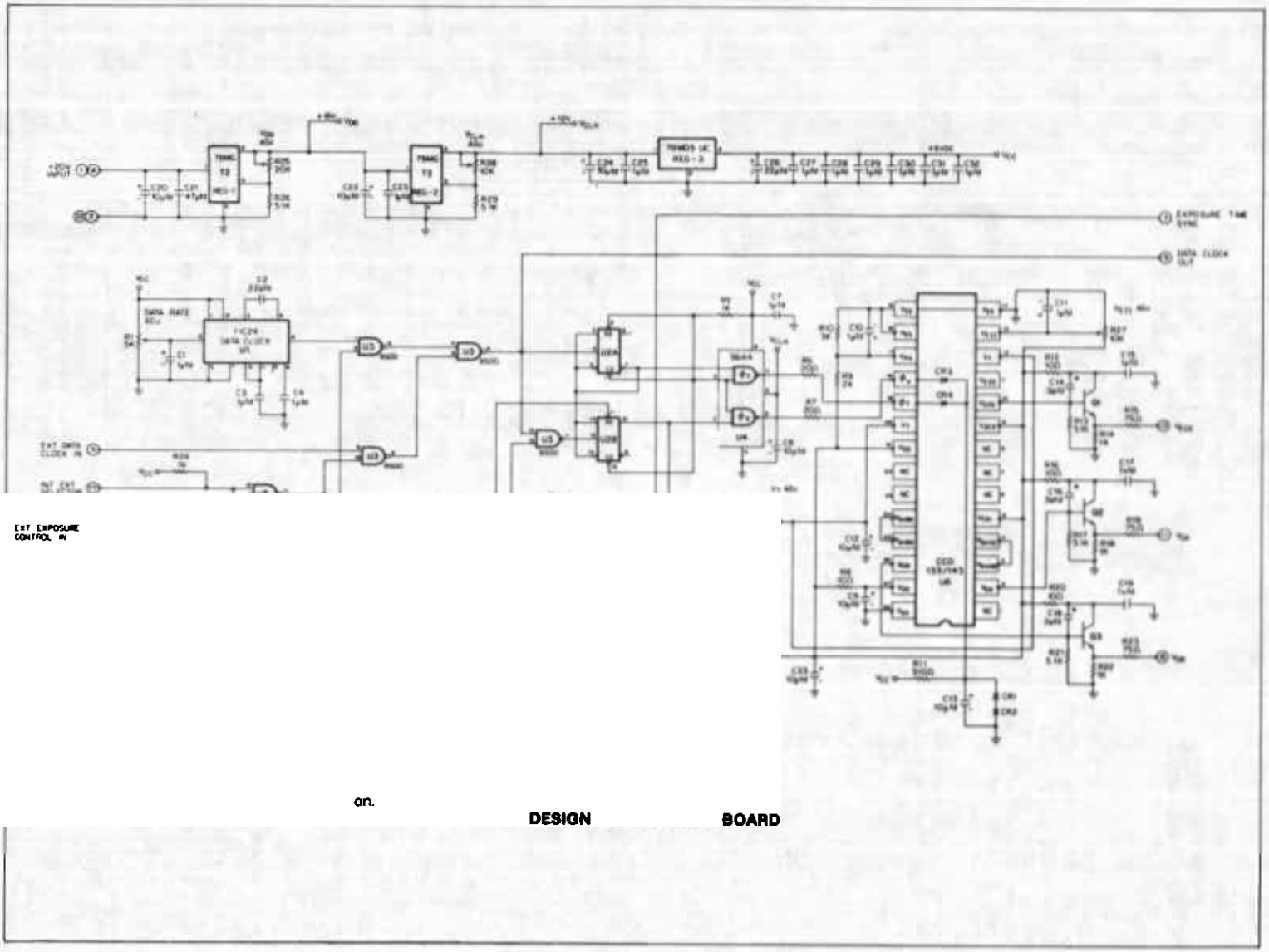
If Finger 17 of the card is held low, the ϕ_T driver will respond to an external data rate clock input on Pin 5 and an external exposure control input to Pin 3. The combined video data rate for the sensor will be equal to the frequency of the clock signal supplied to Pin 5. Sensor exposure intervals are terminated by low-to-high transition on Pin 3.

Connector Figures 7 and 9 provide exposure time and data rate clock output signals for external usage; i.e., for synchronizing an oscilloscope for display of the sensor output signals.

The dc bias voltage applied to the V_T transport register electrodes of the CCD is controlled by R30. This voltage is typically 0.55 times the clock high voltage being supplied to the sensor for best performance. Bias voltage V_{EI} can be set to about 10.5V by R27 to obtain the white reference element output with the video data stream, or it can be increased to V_{DD} to disable the white reference level generating circuitry within the sensor.

NOTICE

This Development Board may not present the optimum test conditions for your design [See application information on page 238], however, redesigned boards are now being engineered for 1987 2nd Quarter availability.



on.

DESIGN **BOARD**

The video signals at the two output ports of the CCD line scan sensor are buffered by emitter followers Q2 and Q3 and then made available on connector Fingers 11 and 15. If long coaxial cables are wired to the outputs, the cables should be terminated in 75 ohms for best frequency response. The cable terminations will reduce the video signal amplitude by one-half.

The sensors end-of-scan output is also buffered by an emitter follower and is then made available on Pin 13. This signal can be amplified and clipped for use as a system synchronizing pulse if desired.

NOTE
1.
2.
3.
4.
5.

Linear Scan CCD Cameras

Fairchild Weston's linear scan cameras are rugged, solid-state instruments incorporating selected advanced-technology sensors.

Linear cameras are used for document scanning in facsimile reproduction, optical character recognition and computer data input systems; for non-contact measurement and automated inspection systems in metal-working, plastics and food processing industries; for control in web-manufacturing situations; and for a great diversity of other industrial, commercial and scientific laboratory applications.

FAIRCHILD WESTON

CCD IMAGING DIVISION

CAM/CCD1000 Series Line Scan Cameras
CAM/CCD1200R 512 Element
CAM/ CD1300R 1024 Element
CAM/CCD1500R 2048 Element

FEATURES

- Small, compact sealed enclosure
- Well suited for use in rugged industrial environments
- All solid state
- Utilizes CCD Sensor: 512, 1024, 2048 resolutions available
- Remote operation (over 200 cable ft.)
- Water jacket compatible for high termperature operation
- Two clock inputs control camera
- No geometric distortion
- 1000:1 dynamic range
- Electronically variable data rate and exposure time
- Accepts C-Mount or 35mm lenses
- Video data rates up to 20 MHz
- Scan rates up to 40,000 lines/second

DESCRIPTION

The CAM/CCD 1500R with a 2048 element array requires a 35mm camera lens. The 512 and 1024 element array lengths (CAM/CCD 1200R and CAM/CCD 1300R) are compatible with C-mount lens (below).

The small sealed enclosure permits the camera to be used in systems where space is limited The camera can be installed in a water jacket when necessary for environmental protection, and can be located more than 200 cable feet away from a control unit/power supply. A C-mount lens adaptor is standard for the CCD1200R and CCD1300R cameras; a 35mm bayonet lens adaptor is standard with the 2048 element model CCD1500R.

Fairchild Weston Systems, Inc. CCD Imaging Division
810 W. Maude Ave., Sunnyvale, California 94086
(408) 720-7600, TWX 910-373-2110

Only two clock signals input through high noise immunity differential line receivers are required for control of the line scan function in the camera. A data rate clock, which can have

and camera. Twisted pair clock wiring can be used for most camera applications; shielded twisted pair cabling is recommended in electrostatically and electromagnetically noisy environments.

The cameras require power supply inputs of +5 and +15 Vdc. Internal regulators and filters provide noise immunity for the bias voltage inputs. Separate force and sense lines allow control of supply voltages and ground potentials at the camera end of long cables.

Two time-division multiplexed analog video outputs are available from coaxial connectors on the camera, at a 75 ohm source impedance. The output video data rate, when meas-

processors are required for systems recognizing gray-scale.

FUNCTIONAL DESCRIPTION

As is shown by the block diagram, the circuitry within the camera is comprised of logic and driver control of the CCD image sensor, the sensor itself, video buffers and power supply filters. An infra-red reject optical filter and lens mounting adaptor are included in the enclosure.

Image Sensor

The Charge Coupled Device line scan image sensor used in the camera is a monolithic component containing a single row of image sensing elements (photosites or pixels), two analog transport shift registers, and two output sense amplifiers. Light energy falling on the photosites generates electron charge packets which are proportional to the product of exposure time (1 ÷ line scan frequency) and incident light intensity. The photosite charge packets are transferred in parallel to the two analog transport registers in response to an exposure time clock signal input into the camera. The transport registers, in response to the data rate clock, deliver the packets in sequence to an integrated charge sensing amplifier where they are converted into proportional video signal voltage levels.

The model CCD1200R camera uses a selected version of the 512 element Fairchild CCD153 sensor; the model CCD1300R camera uses a selected version of the 1024 element CCD133 sensor; and the model CCD1500R uses a selected version of the 2048 element CCD143 sensor.

RUGGEDIZED CAMERA SPECIFICATIONS

Camera	CCD1200R	CCD1300R	CCD1500R
Sensor	CCD153 512 × 1 Element Array	CCD133 1024 × 1 Element Array	CCD143 2048 × 1 Element Array
Photo Element Size	13 μm × 13μm Located on 13 μm centers		
Geometric Distortion	Determined by lens selected		
Dynamic Range	Typically better than 1000:1, excluding clock coupling		
Dark Signal Non-Uniformity (DSNU)	50 mV P-P max. at an integration time of 8.33 ms and $T_A = 25°C$		
Photoresponse Non-Uniformity (PRNU)	100 mV P-P max. @ 1.0 V_{out}, measured at $T_{INT} = 8.33$ ms, $T_A = 25°C$, using a daylight fluorescent light source		
Saturation Exposure	Typically 0.67 $\mu J/cm^2$, using a daylight fluorescent lamp light source		
Saturation Signal Voltage	2 V P-P typical, 1 V P-P minimum		
Spectral Response	The camera includes a Corning 1-75 filter		
Video Data Rate	20 M pixels per second maximum (typical)		
Exposure Time (Min)	26 μS	52 μS	103 μS
Scan Rate (Max) Lines/Second	38 K	19 K	9.7 K

Maximum usable exposure time is limited by the dark signal level developed during the integration time. Dark signal level is an exponential function of camera and (consequently sensor) temperature: dark signal level doubles for each 6-8°C rise in temperature. Dark signal level also increases linearly with exposure time.

The key advantages of Fairchild's isoplanar buried channel CCD sensors for use in the line scan cameras include high data rate capability, high charge transfer efficiencies, low noise, relatively small die sizes, and geometrically precise construction.

Logic and Drivers
Differential line driver input signals are converted into TTL level voltages by the line receivers, and then amplified and shaped for control of the image sensor clock inputs. Single-ended TTL clock inputs can be used if the negative differential input is biased at + 1 V; this technique is recommended only for short cable clock inputs and/or relatively slow video data rate operation.

The frequency of the data rate clock input signal determines the rate at which charge packets are transported along the CCD analog shift register.

Valid Video data from odd-numbered sensor photosites becomes available on video output 'A' within 20ns following alternate rising edges of a data rate clock.

Valid Video data from even-numbered sensor photosites becomes available on video output 'B' within 20ns following interluring alternate riding edges of the data rate clock.

A positive exposure control input signal causes accumulated photosite data to be transferred within the CCD to the analog transport registers for readout under control of the data rate clock The interval between exposure control inputs is the sensor exposure time.

As is noted in the timing diagram, the exposure control pulse input width is unimportant for camera operation. The data rate and exposure control inputs need not be synchronized. The only timing restriction is that the interval between exposure control input signals should be greater than the camera resolution (# of elements) times 1/video data rate to prevent addition of old and new charge packet data in the CCD registers.

Video Output Buffers
Sensor video is buffered by two independent unity-gain 75 ohm output impedance buffers to become the camera video outputs. The video signals ride on a dc level of about 4 volts above ground. External processing circuitry can be used to demultiplex the two video signals. The amplitude of each video signal will typically be 1 V P-P at sensor saturation; the video signal waveforms are sampled and held continuous signals with a small high-frequency sampling clock content.

Optical Components
Each photosite in the sensor is 13 microns (0.51 mils) square. Total active array length is 3.3 mm (.131 inches) for the model CCD1200R, 13.3 mm (.52 inches) for the model CCD1300R, and 26.6 mm (1.04 inches) for the model CCD1500R.

The 512 and 1024 element array lengths are compatible with C-mount lens. The 2048 element array should be used with a 35 mm film camera format lens. Various focal length lenses can be provided by Fairchild as camera accessories.

When ordering, specify device type LENS25C for 25 mm; LENS50C for 50 mm, standard C-mount lens.

A Corning type 1-75 infra-red absorption filter is made a part of the standard cameras. The filter transmission convolved with the spectral responsivity of a silicon CCD sensor gives the camera a response ranging from about 400 to 800 nm, with a peak response at about 700 nm.

BLOCK DIAGRAM

EXPOSURE PULSE

EXPOSURE SYNC

CAMERA CONNECTIONS

J1

Pin	
6	Data Rate Clock (MC1), 20 MHz MAX Differentially Received
13	Exposure Control Clock Pulse (XTO), 25ns Min. Width, Differentially Received
5	+5 V @ 500 mA MAX
12	+15 V @ 250 mA MAX
8	Ground
15	Data Rate Clock (MC2), Differentially Driven
7	Exposure Sync (XT2), Differentially Driven
14	Video A, 75 Ohm Source Impedance
4	Video B, 75 Ohm Source Impedance
11	+5 V Sense
2	+15 V Sense
9	Ground Sense
3	
10	
1	

J4

VIDEO B

Diameter 2.25"

Length 5 125" Without Lens

EXPOSURE TIME

VIDEO A

VIDEO B

NOTES:

1. N = Number of elements in the array, i e, 512, 1024, or 2048.
2. LINE RATE = At least 25ns wideth, may be asynchronous and should not occur while video data is being clocked out
3. DR = 20 MHz MAX. Data rate out equals data rate in plus 20ns (typical camera propagation time) and any transmission line delay
4. LINE SNYC = Time interval between leading edges determines integration time.

ORDERING INFORMATION

When ordering, specify device type
CCD1200R 512 × 1 Element Array
CCD1300R 1024 × 1 Element Array
CCD1500R 2048 × 1 Element Array
CAM if you want camera only.
CCD if you want camera, control box and cable.

STATEMENT OF LIMITED WARRANTY

Within 12 months of receipt by the customer, Fairchild Weston CCD Imaging Division will repair or replace at our option the camera product if any part is found to be defective in materials or workmanship. Labor costs are included. In U.S., please *contact a Camera Repair Center by phoning (408) 720-7600,* or 081 65/618-0 in West Germany.

SPECIALS

All Fairchild Weston CCD cameras are very flexible and can be modified to suit unusual applications. Fairchild is interested in developing and manufacturing customized versions of the basic camera for volume purchasers and is willing to assist low-volume purchasers in development of custom modifications by provision of design and applications engineering assistance.

FAIRCHILD WESTON

CCD IMAGING DIVISION

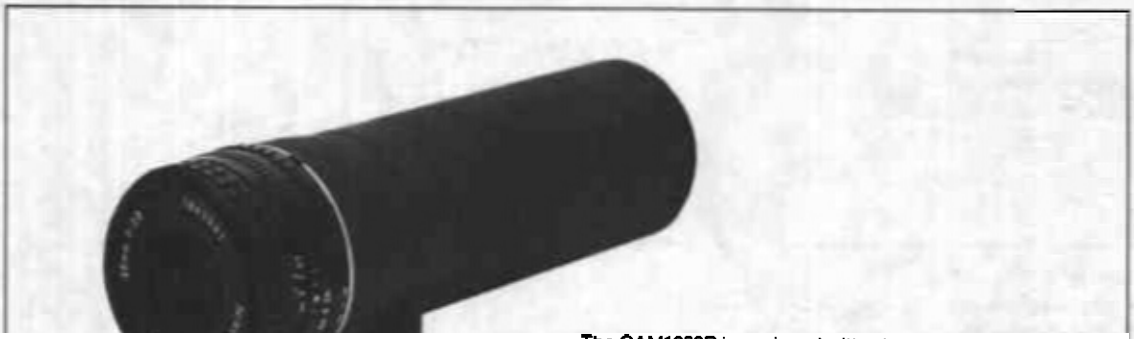
CAM/CCD1600R
Line Scan Camera and
Line Scan Camera System

3456 - ELEMENTS

CAM1600R FEATURES

CAM1600R

Fairchild Weston Systems, Inc. CCD Imaging Division.
810 W. Maude Ave., Sunnyvale, California 94086
(408) 720-7600. TWX 910-373-2110



The CAM1600R is equipped with a bayonet mount for 35mm SLR film camera lenses, allowing selection from a wide choice of commercially available optics for various applications. An infrared-rejecting optical glass filter is bonded into the image input path to give the camera a near-photopic spectral response characteristic, and to provide protection against environmental dust and dirt.

DESCRIPTION

Fairchild Weston Model CAM1600R is a versatile industrial-grade line scan camera with a resolution of 3456 elements. The CAM 1600R is designed for use in high-resolution document scanners, high-accuracy automated measurement and process control systems, fine-detail automated surface inspection systems, and in other office, industrial, and laboratory applications.

The Model CCD1600R is a line scan camera system comprised of a CAM1600R, a CB1000R camera control and interface unit, and a cable set. The CB1000R includes a versatile timing signal generator for control of the camera, an analog module for processing of the camera video output, a pixel locator module for interfacing the camera and digital processing equipment, and a power supply module. The system offers purchasers the inherent economic and technical advantages of a ready-to-operate factory-calibrated instrument.

The primary output of the CAM1600R line scan camera is an analog waveform showing the spatial distribution of incident illumination intensity along a scanned line. Conversion of the optical input into an analog signal is accomplished by a *monolithic CCD image sensor containing 3456 photo* detecting elements aligned in a single row. The CAM1600R high-resolution line scan camera can be readily employed to accurately measure the width and/or edge locations of stationary objects or material in web form. If an object is transported past the field of view of the camera, a complete two dimensional image of the object can be constructed from the series of line-scanned data. The CAM1600R is consequently recommended for use in acquiring two-dimensional images for objects carried by conveyors, for high-resolution facsimile-type scanning of documents transported past the camera, for edge location and/or surface inspection systems in web manufacturing processes, and for non-contact, high-resolution measurement of the width of stationary objects.

Two input clock signals control the video data rate and line scan rate of the CAM1600R. High noise immunity for the input clock signals is provided by differential line receivers, permitting unshielded twisted-pair wiring to be used for most installations. Differentially driven clock signal outputs can be used to synchronize associated equipment for processing camera-acquired data. The CAM1600R requires power supply inputs of +5 and +15V dc. The video output of a CAM1600R for each line scanned is a single sampled-and-held waveform providing image brightness information for each of the 3456 photosites in element-sequential format. The analog video waveform also contains, as shown on the timing diagram, outputs from two sets of eight black-reference elements which provide a measure of the dark current of the sensor. A coaxial connector provides access to the analog video at a 75 ohm source impedance level.

The control unit of the CCD1600R system allows the camera data and line scan rates to be controlled by either internal variable frequency oscillators or by external sources of TTL-level signals. The line rate can be locked to twice the power line frequency for convenience when the camera illumination is derived from line driven florescent or incandescent lamps. The control unit provides a ground referenced gain normalized dc coupled analog video output, and a binary video output with an adjustable threshold voltage. Run length encoded transition address data and other digital information with easy-to-use protocols are available for camera-computer interfacing. The control unit of the CCD1600R also includes a power supply module operating from 110/220 VAC, 47-63 Hz inputs.

The CAM1600R is equipped with a bayonet mount for 35mm SLR camera lenses allowing selection from a wide choice of commercially available optics for various applications. An infrared-rejecting optical glass filter is bonded into the image input path to give the camera a near-photopic spectral response characteristic, and to provide protection against environmental dust and dirt.

CAM1600R SPECIFICATIONS — Measured at T_A = 25°C, data rate = 1 MHz, Line rate = 120 Hz, daylight fluorescent light source, terminated video output (75 ohm), unless otherwise noted.

Sensor — Selected Fairchild Weston CCD151.

Resolution — 3456 elements per line.

CTF — >60% @ 3456 lines per scan width.

Spectral response range — 400 to 700 nm.

Sensor photoelement dimensions — 7 x 7 microns on 7 micron centers along the array.

Saturation signal amplitude — ≥500 mVp-p.

Responsivity — ≥1.5 volts per $\mu J/cm^2$.

Photo response non-uniformity — ≤10% of output signal amplitude.

Dark signal non-uniformity — ≤20 mVp-p (See Note 1).

Maximum video data rate — ≥5M elements/second (See Note 2).

Maximum line scan rate — Video data rate divided by 3514, i.e., 711 Hz at 2.5 MHz data rate (See Note 2).

Power input — ≤3.25 W (250mA @ +5Vdc, 125mA @ +15Vdc).

Dimensions — See figure.

Weight — <18 oz.

Environmental Conditions

Operating Ambient Temperature Range — 0 to 60° C.

Storage Temperature Range — -40 to +100° C.

Shock: <500G any axis.

Vibration — 0-2000Hz, 20G, any axis.

CCD1600R SYSTEM SPECIFICATIONS

Includes — CAM1600R, CB1000R, and cable set.

Camera data rate — Internal: 1 to 3 MHz; External: .01 to 5 MHz

Camera line rate — Internal: 100 Hz to data rate divided by 3514 (e.g., 1.4K lines/second @ 5 MHz data rate). Line sync, twice power line frequency. External: 10 Hz to data rate divided by 3514.

Analog video output — 0-1V p-p sampled-and-held waveform, dc coupled, white positive, 75 ohms, BNC connector, switch-selectable AGC.

Binary video output — TTL-level, BNC connector, white positive, adjustable threshold.

Digital outputs — BNC connectors, TTL-levels. Line sync, video valid, data rate clock.

Processed digital data outputs — TTL-levels, 50 pin connector. Transition addresses, 11-bit words. Transition counts, 8-bit words. Handshakes.

VIP interface outputs — TTL-levels, 15 pin conector. Valid video, line sync, data rate clock.

Timing signal inputs: — TTL-levels, BNC connectors. Data rate and line rate clocks.

Operating mode select inputs — TTL-levels, 50 pin connector. Run, scan, computer control.

CB1000R panel controls — Potentiometers: Binary video threshold data and line rates. Switches: Power (on/off), video AGC (on/off), data rate clock (internal/external), line rate clock (internal/AC sync/external).

Power main input — 110 or 220 VAC, 47-63 Hz.

NOTES:
1) Dark signal non-uniformity should be expected to double for each 6-10° C increase in camera temperature, and to increase linearly with exposure time = 1/line rate.
2) Minimum useful data and line rates are determined by integration of dark signal during integration period.

CAM1600R TIMING DIAGRAM

NOTE: ① TIMING RELATION DEPENDS UPON THE INTERNAL SYNCHRONIZATION CIRCUITRY CONSEQUENTLY LINE SYNC SHOULD BE USED FOR EXTERNAL PROCESSING. DELAY SHOWN IS 1-2 DATA RATE CLOCK CYCLES.

FUNCTIONAL DESCRIPTION — CAMERA

The electronics provided within the CAM1600R include digital timing and CCD clock driver circuitry, components for CCD biasing, the CCD sensor, and a buffer for driving the analog video output cable. A bayonet lens mount, a spectral response filter, and a removable bracket for attachment of the camera to a tripod or other fixture are included in the rugged camera enclosure

IMAGE SENSOR

The image sensor used in the CAM1600R is a selected Fairchild Weston CCD151. This Charge Coupled Device (CCD) is a monolithic integrated circuit containing 3456 photo sensing elements (sometimes called photosites or pixels), two charge-coupled analog shift registers, and an output charge sensing preamplifier The 3456 photosites are arranged in a single row. Light energy absorbed within the photosites generates free electrons which are accumulated into photosite charge packets during integration periods The quantities of electrons accumulated in the photosite charge packets are linearly proportional to the product of the localized incident illumination intensity multiplied by the exposure time

An exposure interval is terminated by input of an exposure clock low-to-high transition. This input causes packets of charge to be transferred from the 3456 photosites into CCD shift register cells. The charge packets are then sequentially transported, in response to the data rate clock input of the camera, to a charge sensing amplifier where they are converted into proportional video signal voltage levels. A following on-chip MOS switching circuit and source follower provides a sample-and-hold analog video waveform output from the CCD.

The CCD151 sensor used in the CAM1600R camera is manufactured with Fairchild Weston's advanced buried-channel CCD technology which provides low noise, relatively small die size for a high-resolution sensor, high charge transfer efficiency, and precise photosite geometries.

OPTICAL CONSIDERATIONS

The optically sensitive area of the CCD is a row of 3456 photosites spaced on 7 micron centers Each photosite is a 7 micron by 7 micron square The photosites are contiguous along the line scan axis of the sensor — there is no optically inactive area separating the individual sites. The total length of the scanned line on the sensor surface is 3456 x 7 microns, or 24 2 mm.

An infrared rejecting filter fabricated from Schott type BG-38 glass is secured into the enclosure between the lens mount and sensor. The filter's spectral transmission characteristic of the filter convolves with the spectral responsivity of the CCD sensor to give the camera a spectral sensitivity extending from 400 to 700 nm, and a symmetrical response curve approximating the photopic characteristic of human eyes. The CAM1600R is equipped with a bayonet lens mounting ring which mates with 35mm camera format lenses. Cameras with either Olympus- or Nikon-compatible mounts are available. Various focal length lenses can be obtained from Fairchild.

LOGIC AND DRIVER CIRCUITS

Differential line receiver circuits are included in the camera to realize good noise immunity for the Data Rate and Line Rate clock signal inputs. The receiver circuits are Fairchild type 9637, or equivalent. Operation with single-ended TTL-level clock inputs can be used for short cable lengths by biasing the negative input for each clock at +1V.

The logic and driver circuits within the camera ensure that properly synchronized, shaped, and timed clock waveforms are given to the CCD. The frequency of the line rate clock input determines the line scan rate of the camera. The interval between successive line rate clock inputs is the sensor exposure time. The frequency of the data rate clock input determines the rate at which photosite data is sequentially delivered by the analog video camera output. One photosite signal is provided at the camera output for each cycle of the data rate clock input.

The rising edge of a line rate input clock terminates an exposure time by transferring the accumulated data from the CCD photosites into the CCD transport registers. The transport registers move the data in photosite increments to the CCD output amplifier. The only timing constraint for the two input clocks is that the interval between line rate inputs should be greater than 3514 cycles of the data rate clock to allow complete read-out of the previously transferred line

VIDEO OUTPUT SIGNAL

Sensor video is buffered by a unity gain amplifier to drive the analog video output of the camera with 75 ohm source impedance. The video signals at the output terminated in 75 ohms will have a typical amplitude of 600m Vp-p at sensor saturation riding on a dc level between +2 and +5V. A coherent sampling clock signal with an amplitude of about 50 mVp-p is combined with the analog video — this can be removed by a low-pass filter or resampling circuit within the equipment using the camera data.

FUNCTIONAL DESCRIPTION — CAMERA CONTROL UNIT

Model CB1000R is a power supply and control unit specifically designed for use with the CCD1600R and other line scan cameras.

The timing signal generator in the CB1000R includes an internal clock oscillator which can drive the camera at data rates from below 1 to above 3MHz. A switch and BNC connector allow the camera data rate to be controlled by an external source of TTL-level input square waves. The line scan rate of the CCD1600R camera driven by the CB1000R can be locked to twice the power line frequency (120 lines per second with 60Hz power input), controlled by an input TTL-level clock, or controlled by an internal variable-frequency oscillator. The timing signal generator includes a lockout logic circuit which insures that the selected data rate and line scan rate are compatible

A video processor within the CB1000R establishes ground as a reference level for the camera output in the dark, and provides gain normalization so that the output signal level is +1 0V when the camera image sensor is illuminated to 90% of saturation. The video processor also provides a Binary Video signal which is TTL TRUE only when the analog video is above an adjustable threshold voltage.

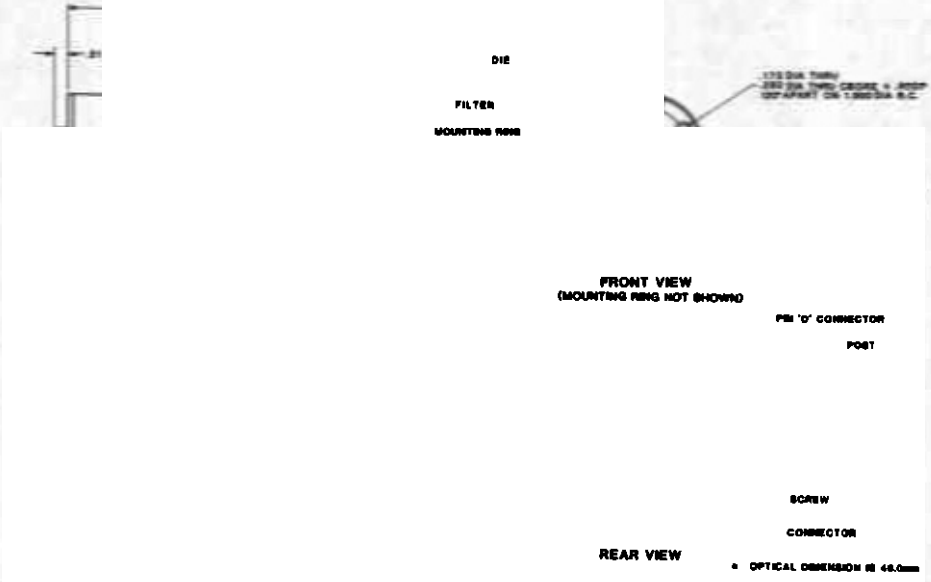
The CB1000R also includes a "pixel locator" which provides FIFO-stored address information indicating photosite locations where binary video transitions from black-to-white, and vice versa, and another set of bit-parallel words indicating in binary coded format the number of binary video transitions occurring in selected camera line scans. This pre-processed digital data, which dramatically simplifies interfacing of the camera subsystem to a microprocessor or computer for many applications, is accessed and controlled by several handshake input and output signals

Power input to the CB1000R can be 110 or 220 VAC, 47-68Hz.

The CB1000R is intended for bench-top installation. All operator controls, and I/O connectors, are located in functional groupings on the front panel for convenience.

MECHANICAL DIMENSIONS

(NOTES: ALL DIMENSIONS ARE IN INCHES UNLESS SPECIFIED)



GNDS	GNDF
+5VS	+5VF
LINE RATE-	LINE RATE+
DATA RATE IN-	DATA RATE IN+
LINE SYNC-	LINE SYNC+
DATA RATE OUT-	DATA RATE OUT+

ORDER INFORMATION AND OPTIONS

Line Scan Camera System — Comprised of a 3456-element line scan camera, a camera control unit, and an interconnection cable set. To order, specify MODEL CCD1600R.

Line Scan Camera Only — Industrial-grade 3456-element line scan camera only with Olympus bayonet lens holder. To order, specify MODEL CAM1600R.

Control Unit and Cable Set Only — A control unit which is set up for operation of a 2048-element line scan camera as shipped. Field modifications are required within the unit for performance optimization when used with a specific CAM1600R camera. To order, specify MODEL CB1000R.

Lenses — Bayonet-mount lenses suitable for use with CAM1600R cameras with local lengths of 25 or 50 mm. To order, specify MODELS LENS25B or LENS50B, respectively.

Cameras with Nikon lens mount — Consult factory.

STATEMENT OF LIMITED WARRANTY

Within 12 months of receipt by the customer, Fairchild Weston CCD Imaging Division will repair or replace at our option the camera product if any part is found to be defective in materials or workmanship. Labor costs are included. In U.S., please contact a Camera Repair Center by phoning (408) 720-7600, or 081 65/618-0 in West Germany.

SPECIALS

All Fairchild Weston CCD cameras are very flexible and can be modified to suit unusual applications. Fairchild is interested in developing and manufacturing customized versions of the basic camera for volume purchasers and is willing to assist low-volume purchasers in development of custom modifications by provision of design and applications engineering assistance.

FAIRCHILD WESTON

CCD IMAGING DIVISION

CB1000R Controller for Line Scan Cameras

CB1000R FEATURES

- Controls Fairchild Industrial Line Scan Cameras:
  - CAM1200R, 512 x 1 elements
  - CAM1300R, 1024 x 1 elements
  - CAM1500R, 2048 x 1 elements
  - CAM1600R, 3456 x 1 elements***
- Fully-integrated subsystems are available.
- Internal/external data rate control.

***consult factory.

CB1000R CONTROLLER

Fairchild Weston Systems, Inc. CCD Imaging Division.
810 W. Maude Ave., Sunnyvale, California 94086
(408) 720-7600, TWX 910-373-2110

and power supply unit
irchild Models CAM1200R,
1600R industrial-grade line
a CB1000R and one of the
ntegrated line scan camera
in laboratory, automated
lodel numbers CCD1200R,
1600R subsystems, respec-
solutions of 512, 1024, 2048

gnal generator, an analog
and a line-driven power
generator allows the video

e changes in
without notice.

data rate of the attached camera to be controlled by an internal variable-frequency oscillator or by an input TTL-level clock signal; allows the line scan rate of the camera to be controlled by an internal variable-frequency oscillator, by an input clock signal, or locked to twice the power line frequency; and provides other useful time signal outputs. The analog video processor provides a 0-1 Vdc-coupled analog video output at a 75 ohm source impedance level, a switch-selectable video AGC function, a binary video (black/white) output with adjustable comparison voltage, and an output signal indicating that the camera is being illuminated to near-saturation level. The pixel locator functions include output of binary-coded data showing the number of binary video transitions occurring in scanned lines, and the pixel addresses where transitions occur, using easy to implement handshake communication protocols for computer-system interfacing. The power supply module, with 47-63Hz, 110 or 220 VAC (nominal) fuse-protected inputs, provides the regulated dc voltages required for camera and CB1000R operation. An additional connector on the CB1000R provides an interface between the attached line scan camera and Fairchild's powerful single-board image processing computer, the VIP-100.

CB1000R SPECIFICATIONS

Compatible with: Fairchild Models CAM1200R, CAM1300R, CAM1500R, CAM1600R Industrial Line Scan Cameras

Camera Control Signals (Differentially driven)

Data Rate Clock
- Internal Oscillator, 1-3MHz
- External Input, 10KHz-20MHz

Line Rate Clock
- Internal Oscillator, 100Hz to a maximum determined by time required to read out one line at selected data rate for selected camera.
- Line Sync, twice the frequency of power line input (e.g., 120Hz with 60Hz input, 100Hz with 50Hz input.)
- External Input, 10Hz to a maximum determined by time required to fully read out one line at selected data rate with selected camera

Camera Supply Voltages — +5 and +15 Vdc, regulated.

Analog Video Output — 0-1 V p-p sampled-and-held waveform, white positive, 75 ohm, BNC connector.

Timing Signal Outputs — TTL-levels, BNC connectors. Binary video, line sync, video valid, data rate clock

Digital Data Outputs — TTL-levels, 50 pin D connector. Transition address words (12-bit parallel), transition count words (8-bit parallel), data ready, FIFO-memory full, transition polarity, saturation warning.

VIP Interface Outputs — TTL-levels, 15 pin D connector. Valid video, line sync, data rate clock.

Timing Signal Inputs — TTL-levels, BNC connectors, used only when external timing controls selected
Data rate clock, line rate clock.

Mode Select Inputs — TTL-levels, 50 pin D connector
Run, scan, computer control

Front Panel Controls and Indicators

Potentiometers; data rate, line rate, binary video threshold

Switches, power (on/off), video AGC (on/off), data rate clock (internal/external), line rate clock (internal/AC sync/external)

LED indicators: Power (+5 Vdc), saturation, mode selected.

Power Input — 110 or 220 VAC, 47-63Hz

Dimensions — See figure.

Installation — Bench top

Operating Ambient Temperature — 0 to 60 °C

CB1000R

PIXEL LOCATOR SWITCH FUNCTIONS

TRANSITION TYPE SELECTION

TYPE \ POS	1	2	3
BLK-WHT	ON	OFF	OFF
WHT-BLK	OFF	ON	OFF
BOTH	OFF	OFF	ON

MINIMUM SEGMENT LENGTH SELECTION*

LENGTH \ POS	4	5	6	7	8
1	OFF	ON	OFF	OFF	OFF
2	OFF	OFF	ON	OFF	OFF
4	OFF	OFF	OFF	ON	OFF
8	OFF	OFF	OFF	OFF	ON

*Segment Length is defined as the minimum width of recorded Binary Video segments between Consecutive Level Transitions whose width is measured in Pixels.

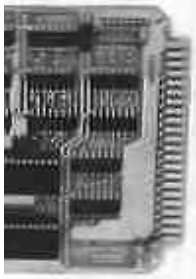
VIDEO PROCESSOR BOARD

TIMING CONTROL BOARD

I/O PIN CONNECTIONS

CAMERA CONNECTOR **DATA CONNECTOR**

PIXEL LOCATOR BOARD



POL

GND

VALID VIDEO

LINE SYNC+

N/C

MC+

VIP BINARY VIDEO

LINE SYNC-

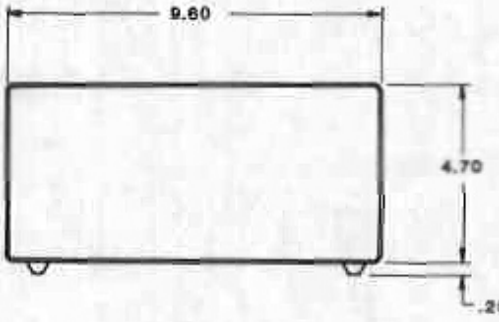
N/C

MC-

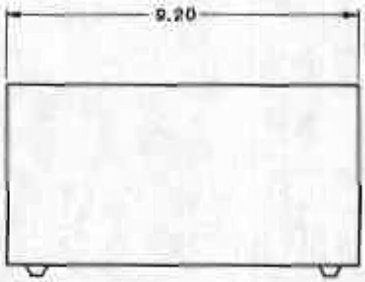
CB1000R MECHANICAL DIMENSIONS

(NOTE: ALL DIMENSIONS ARE IN INCHES)

FRONT VIEW



SIDE VIEW



ORDER INFORMATION

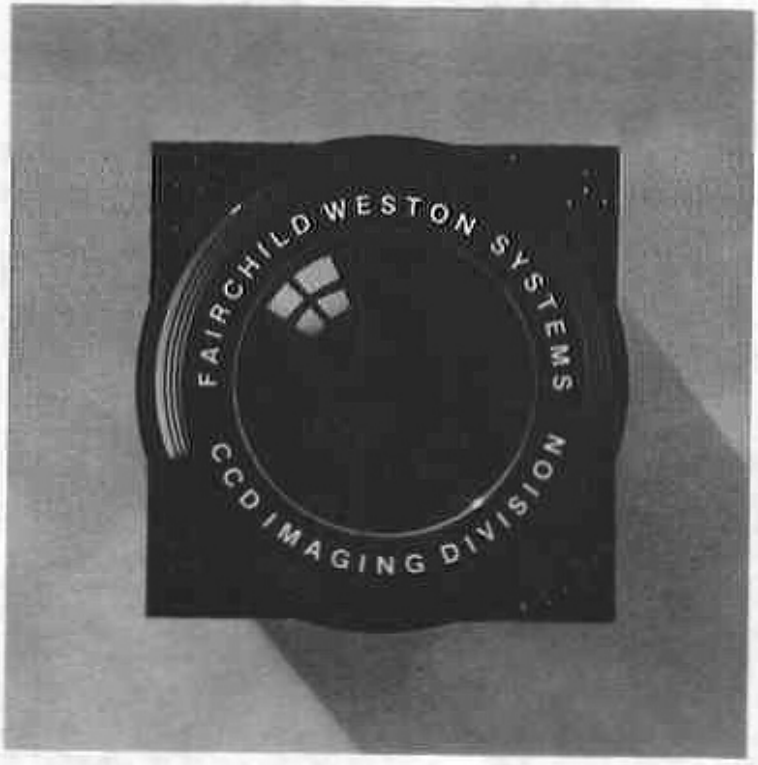
Control Unit — Includes unit with power supply, timing signal generator, video processor, and pixel locator, plus camera-to-control unit cable set and operating manual. Adaptable for control of Fairchild Models CAM1200R, CAM1300R, CAM1500R, or CAM1600R camera. To order, specify FAIRCHILD MODEL CB1000R.

Line Scan Camera Subsystem — Includes CB1000R control unit set up and adjusted for the specific camera. To order, specify FAIRCHILD MODEL:

CCD1200R for 512 element camera system.
CCD1300R for 1024 element camera system.
CCD1500R for 2048 element camera system.
CCD1600R for 3456 element camera system.

STATEMENT OF LIMITED WARANTY

Within 12 months of receipt by the customer, Fairchild Weston CCD Imaging Division will repair or replace at our option the camera product if any part is found to be defective in materials or workmanship. Labor costs are included. In U.S., please contact the Camera Repair Center by phoning (408) 720-7600. In Europe, please phone 061 65/618-0, West Germany.



Area Scan CCD Cameras

Fairchild Weston offers a broad family of solid-state CCD-based monochrome television cameras and camera sub-systems, available in both 525-line RS170A and 625-line CCIR format.

Camera Selector Guide
Solid State TV Cameras

	CAMERA TYPE		
	3000	3002	5000
Sensor Format	~1"	2/3"	~1"
Sensor Measurement (Diagonal)	14.4mm	11.0mm	14.4mm
Sensor Head Dimensions	2 1 Dia. 1 6 Lng.	2.1" Dia. 1.6" Lng	1 3 Dia. 1 5 Lng
Thermo-Electric Cooled Sensor	Yes	No	Yes
Multiple Sense Heads	No	No	Yes
Rugged Moisture Resistant Heads	No	No	Yes

The CCD Imaging Division, pioneer in CCD technology and solid state camera systems, offers a family of solid-state CCD-based monochrome television cameras and camera sub-systems, specifically designed for use in industrial environments.

All cameras meet 525-line RS170A format specifications and 625-line CCIR versions are available in the CCD/CAM 3000 and 3002 series.

Standard Features

- **Interline transfer architecture sensors**
- **488 (V) × 380 (H) pixel element resolution***
- **Environmentally rugged construction**
- **Composite video outputs**
- **Standard RS170 TV system sync**
- **High dynamic range**
- **High signal-to-noise performance**
- **High sensitivity**
- **Variable frame and pixel rates**
- **Gen lock capability**
- **Auto gain control**
- **Remote camera head**
- **Use of standard "C" mount lenses**
- **Spectral response similar to the human eye (photopic)**

Optional Features

All Camera Series

- **Near I.R. response**
- **Non-interlaced scan**
- **Pseudo-interlaced scan**
- **Extended exposure integration**

CCD/CAM 3000 Series Only

- **Blemish-free sensors**
- **CCIR system timing**
- **Asynchronous flash**
- **Synchronous flash**
- **Fiber-Optic faceplate (for 1" Sensor format)**
- **Image intensifier (for 1" CCD format)**

All cameras are engineered for harsh environment surveillance and microscopic operation where acquired image is displayed on standard television monitors, as well as for data input into machine vision processing equipment for automated inspection, robot guidance, object recognition and object location systems.

*except CCD3002 which are 483 (V) × 378 (H)

FAIRCHILD WESTON

CCD IMAGING DIVISION

CAM3000/CCD3000 Solid-State Cameras and Camera Subsystems

with RS170A TIMING

FEATURES

- Small, rugged sense head
- Buried-channel CCD sensor
- 483 × 378 Resolution — CTF > 70% at Nyquist
- No lag, geometric distortion or image burn-in
- Thermo-electrically cooled sensor
- Designed for demanding environments
- Unity gamma
- 525 line, 30 frame internal clock timing meets RS170A specifications
- User selectable timing and format optional
- Genlock and external clock timing control
- C-mount lens holder

CCD3000 SUBSYSTEM

Fairchild Weston Systems, Inc. CCD Imaging Division.
810 W. Maude Ave., Sunnyvale, California 94086
408-720-7600. TWX 910-373-2110

DESCRIPTION

The CAM3000 and CAM3100 are rugged solid-state cameras designed for use in industrial environments. They are general-purpose black-and-white television cameras meeting RS170A standards for timing in a 525-line per frame scanning format. The composite video output of the cameras offers high resolution, wide dynamic range display of images on U S *standard monitors or provide data input into RS170A*-compatible digital machine vision equipment. The camera resolution is 483-lines per frame, 378-elements per line. The monolithic buried channel charge-coupled image sensor is thermo-electrically cooled for optimized camera performance

The CCD3000 series are complete sub-systems comprised of a CAM3000 series control unit and sense head, a power supply unit which also provides BNC-connector access to the most often used camera I/O timing signals, a remote sense head cable and a power supply-to-control unit cable The subsystems offer the inherent convenience and economy of receiving an integrated, ready-to-operate camera system

CAM3000 series cameras can be used as self-contained single-piece units or separated into camera control units and relatively small sense heads connected by a flexible cable The sense heads are designed to withstand the accelerations, shocks, and vibrations which are often encountered in industrial applications and their relatively small size and weight encourage their use on microscopes eliminating the need for expensive mounting brackets and supports

CAM3000F

The CAM3000F and CAM3100F are CAM3000 or CAM3100 cameras modified by incorporation of a fiber-optics faceplate for optical input. A mounting flange and compliant sensor positioning arrangement provide an easy means for interfacing the camera to customer-supplied fiber optics equipment Use of direct bundle-to-bundle fiber optic coupling can dramatically increase the efficiency of image inputs in comparison to lens image-transferring systems The fiber optics faceplate feature makes the CAM3000F ideal for applications in streak camera systems, large-format image intensifier cameras, X-ray and UV image detection systems and in medical, scientific and industrial camera applications

The CAM3000I is a CAM3100F camera which is modified by incorporation of a microchannel plate wafer image intensifier The CAM3000I is intended for industrial, scientific and surveillance applications requiring very low-light-level image detection capability. A C-mount lens holder is provided for optical input into the intensifier faceplate The amplified image output of the intensifier is direct-coupled to the CCD image sensor by coherent, optically-efficient fiber optic bundles

SPECIFICATIONS

CAM3000 AND CAM3100 SPECIFICATION

Scanning Format — Interlaced 483-lines per frame, 378-elements per line (non-interlaced 242 lines per field is a pc strap option).

Read-Out Format — Image data fills horizontal and vertical unblanked portions of frame and line timing intervals as specified by RS170A television standards.

Output Signals
Analog Video: 1.4 Vp-p Composite, 75 ohm, sync negative, white positive, dc coupled.

Timing: TTL-level Vertical and Horizontal Drive, Composite Sync and Blanking, Frame Index, Data Rate Clock. Differential Master Clock.

Input Signals
Differential Master Clock for external frame rate control

Horizontal and Vertical drives for gen-locking, 2-5 Vp-p.

TTL-level clock source selects

Resolution — >60% CTF at 483-lines per picture height, 378-lines per picture width.

Sensor — Monolithic Silicon CCD, 4:3 Aspect Ratio, 14mm image diagonal.

Dynamic Range — Peak Signal (1v): RMS temporal noise in the dark ≥1000:1.

Sensitivity — S:N >20db with faceplate illumination $\geq 10^{-2}$ footcandles. (see figure)

Video Automatic Gain Control — Approximately 10db of additional video gain at low light levels when AGC function is activated.

Cosmetic Performance (T_A = 25°C, AGC Off)

Photo Response Shading Non-Uniformity ≤5% of output for CAM3000, ≤3% of output for CAM3100.

Shading in the dark ≤20 mVp-p

NOTE: The amplitude of dark signal shading non-uniformity and the amplitude of spurious element outputs in the dark should be expected to double for each 5 to 10°C increase in sense head case temperature.

Optical Input — C-mount lens holder (1 inch, 32 thread/inch), standard C-mount 1 inch vidicon type lenses are recommended (see order information). Effective back flange focal length is 17.5 mm, clear thread depth is >0.25 inches (>6.3 mm).

Enclosure — Sense head is O-ring protected, thermally efficient anodized aluminum extrusion.

Dimensions — See figure.

Weight — Sense Head, 8 oz: Sense Head and Control Unit: 2 lbs.

Environmental Conditions — Operating Ambient Temperature: 0-50°C, Acceleration and Shock: Resistant to >100G, any axis.

Power Requirements — <10 W, ±15, +5 Vdc, current controlled 0.8A at approximately 1Vdc.

CAM3000F AND CAM3100F SPECIFICATIONS

CAM3000F and CAM3100F Specifications — Identical to the CAM3000 and CAM3100 with the following exceptions:

Optical Input — Through coherent fiber optic faceplate 0.2 inches in length, cemented in intimate contact with CCD sensor surface. Faceplate uses 6 micron diameter fibers, N.A. = 1.0. Faceplate input is flat and polished. Cameras are shipped with a C-mount lens holder attached.

Cosmetic Performance — Number of blemished elements ≤100 for CAM3000F, ≤10 for CAM3100F, since the faceplate may contain a few open fibers.

Environment — Non-condensing humidity conditions when the sensor temperature is 25°C below ambient.

CAM3000I SPECIFICATIONS

CAM3000I Specifications — Identical to the CAM3000 except for the following:

Image Detector — Comprised of a microchannel plate image intensifier coupled to a CCD sensor by efficient 1:1 image geometry fiber optics.

Spectral Response — "Extended Red" photocathode (see figure).

Sensitivity — S:N >20db with faceplate illumination levels $\geq 10^{-6}$ footcandles.

Automatic Light Control Function — The intensifier gain is automatically reduced as the input light level increases to provide a near-constant output signal level for faceplate illumination levels between 1 and 10^{-5} footcandles (see figure).

Image Burn In — The intensifier photocathode may develop a "burned-in" image if over exposed by excess input light for extended intervals.

Sense Head Weight — 16 oz.

Shock Resistance — Sense head will tolerate up to 20G shocks, any axis.

CCD3000 CAMERA BODY BLOCK DIAGRAM

CCD3000 SENSE HEAD BLOCK DIAGRAM

FUNCTIONAL COMPONENTS

MODEL CAM3000, CAM3100, CAM3000F, CAM3100F and CAM3000I cameras are comprised of a camera control unit and a camera sense head The control unit is identical for all of the camera models; there are significant differences in the sense heads for the three types of cameras Model CCD3000, CCD3100, CCD3000F, CCD3100F and CCD3000I are subsystems comprised of a camera, a power supply unit and two cables. The power supply unit and cables are identical for each camera type.

IMAGE SENSOR

The image sensor employed in the CAM3000-series camera sense head is a selected buried-channel charge coupled device (CCD) manufactured by Fairchild. The interline transfer organization of the sensor provides a resolution of 488-lines per frame, 380-elements per line. Buried channel technology minimizes noise and allows high data rate and high frame rate operation without sacrificing charge transfer efficiency.

For use in a CAM3000 or CAM3100 camera, the CCD is enclosed in a ceramic package sealed with an optical-quality transparent glass cover

For construction of a CAM3000F, CAM3100F or CAM3000I, a coherent bundle of optical fibers 6 microns in diameter and .2 inches in length is bonded to the CCD surface with a hard-setting optical cement The CCD package is then sealed with epoxy. The printed circuit board supporting the fiber optic faceplate sensor is spring loaded so that intimate contact can be made to customer supplied fiber optics with the CAM3000F or CAM3100F, or to the intensifier output in the CAM3000I.

THERMO-ELECTRIC COOLER

The CCD die temperature is reduced to about 20° C below ambient temperature by a Peltier-effect thermo-electric cooler in the sense head. A current-controlled dc power supply input of 0.8 Amp at about 1 V (provided by the power supply unit when a CCD3000, CCD3100, CCD3000F, CCD3100F or CCD3000I is purchased) is required for cooler operation. The cold side of the cooler contacts the CCD package and the hot side of the cooler contacts a heat transfer member which is thermally connected to the finned walls of the sense head enclosure. Sensor cooling reduces the random temporal noise content in the signal output of the sensor and also reduces the dark current non-uniformity or fixed pattern noise content of the sensor signal.

IMAGE INTENSIFIER (CAM3000I ONLY)

Image inputs into a CAM3000I camera are transmitted by fiber optics to a photocathode where photons are converted into electrons Electrons freed from the photocathode are accelerated by electrostatic potentials towards a wafer-type microchannel plate. Gain is achieved within the microchannel plate where each channel acts as a high-gain electron multiplier Electrons exit the plate and strike an output phosphor which re-converts them into photons. A second fiber optic bundle directs the amplified image from the phosphor to the CCD faceplate. The electron-multiplication gain within the intensifier is dependent upon the accelerating electro-static potentials supplied to the intensifier electrodes and can be higher than 10,000:1 at low light-levels. The impedance of the power supply which provides the operating voltages to the intensifier has been designed so that the gain decreases as the average brightness of the image input increases to give a very wide range AGC function to the CAM3000I.

DETAILED DIAGRAM of the CAMERA FRONT-END

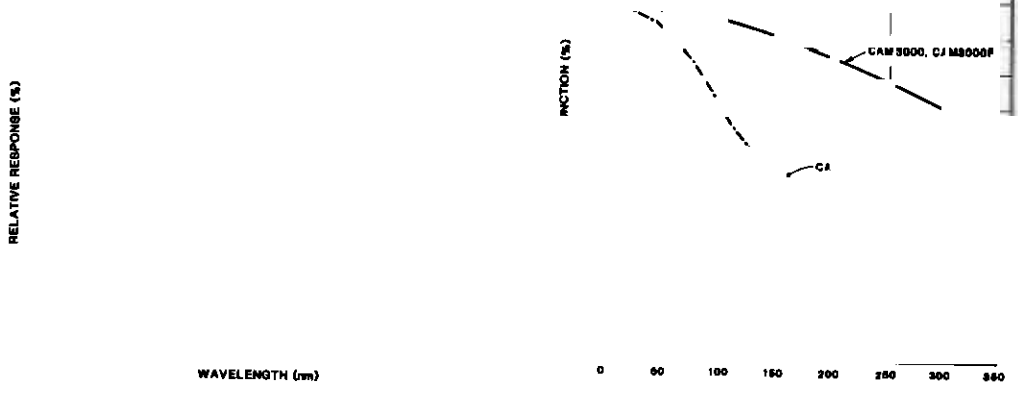
SENSE HEAD CIRCUITRY

The CAM3000 and CAM3100 optical paths include an infrared rejecting filter which gives the camera a near-photopic spectral sensitivity. The CAM3000, CAM3100 and CAM3000I sense heads are protected against dirt and dust by O-ring seals; the CAM3000F and CAM3100F are unsealed for user convenience when employing fiber optic inputs.

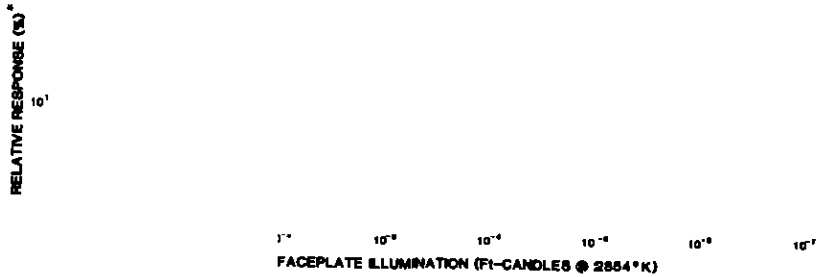
CAMERA CONTROL UNIT

TYPICAL PERFORMANCE CURVES

SPECTRAL RESPONSE



TI



* RELATIVE RESPONSE IS RELATIVE AMPLITUDE OF LOW FREQUENCY WHITE-TO-BLACK TRANSITION IN 90% WHITE SCENE.
** INPUT ILLUMINATION FILTERED WITH BG-38

POWER SUPPLY

I/O PIN CONNECTIONS

GND	
HORIZONTAL DRIVE IN	
HORIZONTAL DRIVE OUT	
VERTICAL DRIVE IN	
TIMING SELECT A	
TIMING SELECT B	
MASTER CLOCK+ IN	
MASTER CLOCK- IN	
MASTER CLOCK+ OUT	
MASTER CLOCK- OUT	
VERTICAL DRIVE OUT	
FIELD INDEX	
T.E COOLER RETURN	

MATING CONNECTOR IS TYPE DB-25S BY TRW OR EQUIVALENT

POWER SUPPLY UNIT

The power supply unit, which is a part of the CCD3000, CCD3000F and CCD3000I sub-systems or which can be ordered separately for use with any of the cameras, contains a linear power supply module, timing signal buffer amplifiers and I/O signal connectors.

Power input is through a fuse-protected recessed male connector. Input voltages of 110 or 220 VAC, ±10% can be selected by an insert switch mechanism. A detachable 3-wire grounding cord with U.S. standard plug is included.

Camera Control Unit

Power Supply Cable

Sense Head

Power Supply Unit

MECHANICAL DIMENSIONS
(NOTE ALL DIMENSIONS ARE IN INCHES)

CONTROL UNITS

SENSE HEADS

SENSE HEAD& CONTROL UNIT FRONT VIEWS

REAR VIEW
CAM3000
CAM3000F
CAM3000I

SENSE HEAD BOTTOM VIEW
CAM3000
CAM3000F
CAM3000I

CAM3000 (DOVETAIL&FRONT PLATE REMOVED)

SCREW THREAD 6-32 ON 2.80 DIA B.C. 4PL

NOTE:

a The spring loaded faceplate will move inward approximately .06 inch in response to an applied force normal to the faceplate of 2 lbs.

CAM3000 I

ORDER INFORMATION

CCD3000 — Includes a CAM3000 camera, a 12 foot (3.6 meter) remote sense head cable, a power supply unit and a power supply-to-control unit cable To order, specify FAIRCHILD MODEL CCD3000.

CCD3100 — Includes a CAM3100 camera, a 12 foot (3.6 meter) remote sense head cable, a power supply unit and a power supply-to-control unit cable. To order, specify FAIRCHILD MODEL CCD3100

CCD3000F — Includes a CAM3000F camera, a 12 foot (3 6 meter) remote sense head cable, a power supply unit and a power supply-to-control unit cable To order, specify FAIRCHILD MODEL CCD3000F

CCD3100F — Includes a CAM3100F camera, a 12 foot (3.6 meter) remote sense head cable, a power supply unit and a power supply-to-control unit cable. To order, specify FAIRCHILD MODEL CCD3100F

CCD3000I — Includes a CAM3000I camera, remote sense head cable 12 foot (3.6 meters) in length, a power supply unit and a power supply-to-control unit cable. To order, specify FAIRCHILD MODEL CCD3000I.

CAM3000 — RS170A Format camera only. To order, specify FAIRCHILD MODEL CAM3000.

CAM3100 — RS170A Format camera only. To order, specify FAIRCHILD MODEL CAM3100.

CAM3000F — RS170A Format camera only with fiber optics faceplate. To order, specify FAIRCHILD MODEL CAM3000F.

CAM3100F — RS170A Format camera only with fiber optics faceplate. To order, specify FAIRCHILD MODEL CAM3100F.

CAM3000I — RS170A Format intensified CCD camera only. To order, specify FAIRCHILD MODEL CAM3000I.

Power Supply Unit — This unit provides ±15, +5Vdc, and the TE cooler current inputs to the CAM3000, CAM3100, CAM3000F, CAM3100F or CAM3000I derived from power line voltages of 110±10 or 220±20/VAC, 45–63Hz. The front panel of the power supply unit provides BNC-connector access to composite blanking, composite sync, vertical drive, and horizontal drive output signals, and horizontal and vertical drive and external clock input signals, plus a convenient connector for interfacing the camera and power supply to the Fairchild VIP100 Video Interface Processor or other auxiliary equipment.

The front panel also supports an AGC off/on switch, a clock source select switch, and a power off/on switch.

A 6' (1.8 meters) cable is provided for interconnection of the camera control unit and the power supply To order, specify FAIRCHILD MODEL PWRSPLY.

Remote Sense Head Cable — Allows sense head to be remoted from camera control unit by a distance of 12' (3.6 meters). Up to 4 CABLAUTOs can be used in series with little degradation in camera performance. To order, specify FAIRCHILD MODEL CABLAUTO.

Lenses — 1" Vidicon type "C"-mount lenses are available in focal lengths of 12.5mm, 25mm, and 50mm To order, specify Models LENS12.5C, LENS25C, and LENS50C, respectively.

Monitor — RS170A monitor. To order, specify FAIRCHILD MODEL MONITOR.

SPECIALS

All Fairchild Weston CCD cameras are very flexible and can be modified to suit unusual applications. Fairchild is interested in developing and manufacturing customized versions of the basic camera for volume purchasers and is willing to assist low-volume purchasers in development of custom modifications by provision of design and applications engineering assistance.

WARRANTY

Within twelve months of delivery to the end customer, Fairchild Weston CCD Imaging will repair or replace, at our option, any Fairchild Weston camera product if any part is found to be defective in materials or workmanship. Please call (408) 720-7600 in the U.S. or 081/65/618-0 in West Germany for information on assignment of a *warranty return number and shipping instructions to ensure prompt* repair or replacement.

CERTIFICATION

Fairchild Weston CCD Imaging certifies that this product will be carefully inspected and tested at the factory prior to shipment and will meet all requirements of the specifications under which it is furnished.

The new Fairchild Weston CAM3000-A solid-state CCD camera, combining the excellent electro-optical performance and very small sense head of the CCD/CAM5000 series with the *Camera Control Unit of the* popular CCD/CAM3000 series, is ideal for industrial testing, medical/scientific imaging and machine vision applications.

FAIRCHILD WESTON

CCD IMAGING DIVISION

CAM3500/CCD3500 Solid-State Cameras and Camera Subsystems

with CCIR TIMING

FEATURES

- Small, rugged sense head
- Buried-channel CCD sensor
- 488×380 Resolution — CTF>70% at Nyquist
- No lag, geometric distortion or image burn-in
- Thermo-electrically cooled sensor
- Designed for demanding environments
- Unity gamma
- 625 line, 25 frame internal clock timing meets CCIR specifications
- User selectable timing and format optional
- Genlock and external clock timing control
- C-mount lens holder

power supply, power and remote sense head cables

- Special modifications available — consult factory

Fairchild Weston Systems, Inc. CCD Imaging Division
810 W. Maude Ave., Sunnyvale, California 94086
408-720-7600, TWX 910-373-2110

DESCRIPTION

The CAM3500 and CAM3600 are rugged solid-state cameras designed for use in industrial environments. They are general-purpose black-and-white television cameras meeting CCIR standards for timing in a 625-line per frame scanning format. The composite video output of the cameras offer high resolution, wide dynamic range display of images on European standard monitors, or provide data input into CCIR-compatible digital machine vision equipment The camera resolution is 488-lines per frame, 380-elements per line. The monolithic buried channel charge-coupled image sensor is thermo-electrically cooled for optimized camera performance.

The CCD3500, CCD3600, CCD3500F, CCD3600F and CCD-3500I are complete sub-systems comprised of a CAM3500, CAM3600, CAM3500F, CAM3600F or CAM3500I camera, a power supply unit which also provides BNC-connector access to the most often used camera I/O timing signals, a remote sense head cable and a power supply to control unit cable. It is recommended that the CCD sub-systems be ordered for low-volume applications because of the inherent convenience and economy of receiving an integrated ready-to-operate camera system

CAM3500, CAM3600, CAM3500F, CAM3600F or CAM3500I cameras can be used as self-contained single-piece units or separated into camera control units and relatively small sense heads connected by a flexible cable The sense heads are designed to tolerate the accelerations, shocks, and vibrations which are often encountered in industrial applications and their relatively small size and weight encourage their use on microscopes without requirement for expensive mounting brackets and supports.

CAM3500F

The CAM3500F and CAM3600F are CAM3500 or CAM3600 cameras modified by incorporation of a fiber-optics faceplate for optical input A mounting flange and compliant sensor positioning arrangement provides an easy means for interfacing the camera to customer-supplied fiber optics equipment. Use of direct bundle-to-bundle fiber optic coupling can dramatically increase the efficiency of image inputs in comparison to normal lens image forming systems for many applications. The fiber optics faceplate feature makes the CAM3500F ideal for applications in streak camera systems, large-format image intensifier cameras, X-ray and UV image detection systems and in other medical, scientific and industrial camera applications.

The CAM3500I is a CAM3600F camera which is modified by incorporation of a microchannel plate wafer image intensifier. The CAM3500I is intended for industrial, scientific and surveillance applications requiring very low-light-level image detection capability A C-mount lens holder is provided for optical input into the intensifier faceplate. The amplified image output of the intensifier is coupled to the CCD image sensor by coherent, optically efficient fiber optic bundles.

CAM3500 AND CAM3600 SPECIFICATIONS

Scanning Format — Interlaced 488-lines per frame, 380-elements per line (non-interlaced 244-lines per field is a pc strap option).

Scan Timing — Frame rate is 25Hz, data rate is 9M elements per second when camera is under control of internal crystal oscillator. Frame rate can be varied from below 5 to above 40Hz (typically >50Hz) when using external master clock input. Camera can be synchronized to external equipment (gen-locked) with horizontal and vertical drive inputs.

Read-Out Format — Image data is centered horizontally and vertically in unblanked portions of frame and line timing intervals as specified by CCIR television standards.

Output Signals
Analog Video: 1.4 Vp-p Composite, 75 ohm, sync negative, white positive, dc coupled.

Timing: TTL-level Vertical and Horizontal Drive, Composite Sync and Blanking, Frame Index, Data Rate Clock. Differential Master Clock.

Input Signals
Differential Master Clock for external frame rate control.

Horizontal and Vertical drives for gen-locking, 2-5 Vp-p.

TTL-level clock source selects.

Resolution — >60% CTF at 488-lines per picture height, 380-lines per picture width.

Sensor — Monolithic Silicon CCD, 4:3 Aspect Ratio, 14mm image diagonal.

Dynamic Range — Peak Signal (1v): RMS temporal noise in the dark ≥1000:1.

Sensitivity — S:N >20db with faceplate illumination $\geq 10^{-2}$ footcandles (see figure).

Video Automatic Gain Control — Approximately 10db of additional video gain at low light levels when AGC function is activated.

Cosmetic Performance (T_A = 25°C, AGC Off)

Photo response shading non-uniformity ≤5% of output.

Shading in the dark ≤20 mVp-p for CAM3500, ≤10mVp-p for CAM3600.

Number of blemished elements ≤20 for CAM3500, ≤5 for CAM3600, where blemished elements are defined as areas exhibiting a spurious response of >50 mVp-p compared to their nearest neighbors at any illumination level. No element will exhibit a spurious response ≥350 mVp-p for a CAM3500, ≥150 mVp-p for a CAM3600.

NOTE: The amplitude of dark signal shading non-uniformity and the amplitude of spurious element outputs in the dark should be expected to double for each 5 to 10°C increase in sense head case temperature.

Optical Input — C-mount (1 inch, 32 thread/inch) holder, standard C-mount 1 inch vidicon type lenses are recommended (see order information). Effective back flange focal length is 17.5 mm, clear thread depth is >0.25 inches (>6.3 mm).

Enclosure — Sense head is O-ring protected, thermally efficient anodized aluminum extrusion.

Dimensions — See figure

Weight — Sense Head, 8 oz; Sense Head and Control Unit: 2 lbs.

Environmental Conditions — Operating Ambient Temperature. 0-50°C, Acceleration and Shock: Resistant to >100G, any axis.

Power Requirements — <10 W, ±15, +5, + 1 Vdc.

CAM3500F and CAM3600F SPECIFICATIONS

CAM3500F and CAM3600F Specifications — Identical to the CAM3500 and CAM3600 with the following exceptions:

Optical Input — Through coherent fiber optic faceplate 0.2 inches in length, cemented in intimate contact with CCD sensor surface. Faceplate uses 6 micron diameter fibers, N.A. = 1.0. Faceplate input is flat and polished.

Cosmetic Performance — Number of blemished elements ≤100 for CAM3500F, ≤10 for CAM3600F, since the faceplate may contain a few open fibers.

Environment — Non-condensing humidity conditions when the sensor temperature is 20°C below ambient.

CAM3500I SPECIFICATIONS

CAM3500I Specifications — Identical to the CAM3500 except for the following:

Image Detector — Comprised of a microchannel plate image intensifier coupled to a CCD sensor by efficient 1:1 image geometry fiber optics.

Spectral Response — "Extended Red" photocathode (see figure).

Sensitivity — S:N >20db with faceplate illumination levels $\geq 10^{-6}$ footcandles.

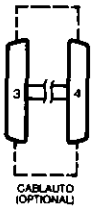
Automatic Light Control Function — The intensifier gain is automatically reduced as the input light level increases to provide a near-constant output signal level for faceplate illumination levels between 1 and 10^{-5} footcandles (see figure).

Image Burn In — The intensifier photocathode may develop a "burned-in" image if over-exposed by excess input light for extended intervals.

Sense Head Weight — 16 oz.

Shock Resistance — Sense head will tolerate up to 20G shocks, any axis.

CCD3500 CAMERA BODY BLOCK DIAGRAM



CCD3500 SENSE HEAD BLOCK DIAGRAM

FUNCTIONAL COMPONENTS

MODEL CAM3500, CAM3600, CAM3500F, CAM3600F and CAM3500I cameras are comprised of a camera control unit and a camera sense head. The control unit is identical for all of the camera models; there are significant differences in the sense heads for the three types of cameras. Model CCD3500, CCD3600, CCD3500F, CCD3600F and CCD3500I are subsystems including a camera, a power supply unit and two cables The power supply unit and cables are identical for each camera type.

IMAGE SENSOR

The image sensor employed in the CAM3500-series camera sense head is a selected buried-channel charge coupled device (CCD) manufactured by Fairchild Weston. The interline transfer organization of the sensor provides a resolution of 488-lines per frame, 380-elements per line. Buried channel technology minimizes noise and allows high data rate and high frame rate operation without sacrificing charge transfer efficiency

For use in CAM3500 or CAM3600 cameras, the CCD is enclosed in a ceramic package sealed with an optical-quality transparent glass cover. For construction of a CAM3500F, CAM3600F, or CAM3500I, a coherent bundle of optical fibers 6 microns in diameter and .2 inches in length is bonded to the CCD surface with a hard-setting optical cement. The CCD package is then sealed with epoxy. The printed circuit board supporting the fiber optic faceplate sensor is spring loaded so that intimate contact can be made to customer supplied fiber optics with the CAM3500F, CAM3600F, or to the intensifier output in the CAM3500I.

THERMO-ELECTRIC COOLER

The CCD die temperature is reduced to about 20°C below ambient temperature by a Peltier-effect thermo-electric cooler in the sense head A current-controlled dc power supply input of 0.8 Amp at about 1 V (provided by the power supply unit when a CCD3500, CCD3600, CCD3500F, CCD3600F, or CCD3500I is purchased) is required for cooler operation The cold side of the cooler contacts the CCD package and the hot side of the cooler contacts a heat transfer member which is thermally connected to the finned walls of the sense head *enclosure. Sensor cooling reduces the random temporal* noise content in the signal output of the sensor and also reduces the dark current non-uniformity or fixed pattern noise content of the sensor signal.

IMAGE INTENSIFIER (CAM3500I ONLY)

Image inputs into a CAM3500I camera are transmitted by fiber optics to a photocathode where photons are converted into electrons. Electrons freed from the photocathode are accelerated by electrostatic potentials towards a wafer-type microchannel plate. Gain is achieved within the microchannel plate where each channel acts as a high-gain electron multiplier. Electrons exit the plate and strike an output phosphor which reconverts them into photons. A second fiber optic bundle directs the amplified image from the phosphor to the CCD faceplate. The electron-multiplication gain within the intensifier is dependent upon the accelerating electro-static potentials supplied to the intensifier electrodes and can be higher than 10,000:1 at low light-levels The impedance of the power supply which provides the operating voltages to the intensifier has been designed so that the gain decreases as the average brightness of the image input increases to give a very wide range AGC function to the CAM3500I.

SENSE HEAD CIRCUITRY

The sense heads contain, in addition to the CCD image sensor and thermo-electric cooler, (plus intensifier and high voltage supply in the CAM3500I) circuitry for generating the high-frequency clock signals for control of the CCD and a buffer for the sensor video output signal. All other CCD timing and drive electronics, supply and bias voltage regulators, and video processing circuits are contained in the camera control units.

DETAILED DIAGRAM of the CAMERA FRONT-END

MICROCHANNEL
PLATE (MCP)

The CAM3500 and CAM3600 optical paths include an infrared rejecting filter which gives the cameras a near-photopic spectral sensitivity. The CAM3500, CAM3600 and CAM3500I sense heads are protected against dirt and dust by O-ring seals; the CAM3500F and CAM3600F are unsealed for user convenience when employing fiber optic inputs.

CAMERA CONTROL UNIT

The camera control unit houses three pc cards performing the functions of camera and sensor timing control, CCD drive and video processing, interconnected by two pc mother boards. Camera timing is normally controlled by an internal 17.9375 MHz master clock oscillator located on the drive board. The frequency of this oscillator is controlled by a phase-locked loop circuit when the camera timing is "gen-locked" to external vertical and horizontal drive or composite video sync inputs. A vertical drive input or a vertical drive separated from composite inputs is required to establish frame sync in a gen-lock mode. An external master clock signal can be used for variable frame-rate operation.

Timing waveforms for sensor drive and sync signals for the formation of CCIR composite video are derived from the master clock signal. These signals are then fed to the drive board where the TTL level signals are altered to CCD drive level signals required to operate the sensor. From the drive board, sensor clocks are fed through the 31-pin D connector to the sense head and the composite sync signal is forwarded to the video processor board.

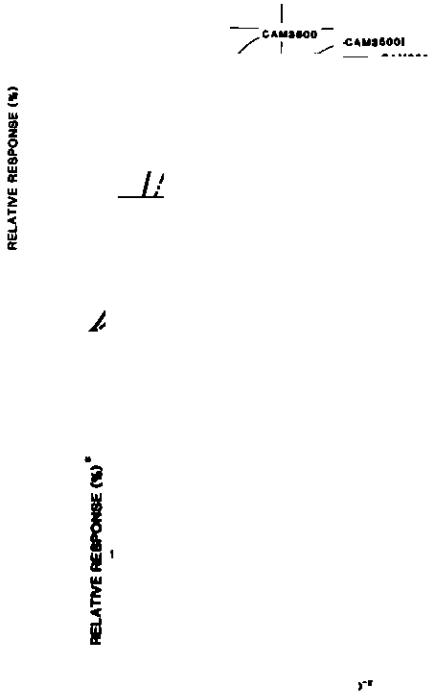
The video processor receives sensor video from the CCD in the sense head. The video is line-clamped, amplified, and blanked with composite blanking from the logic board and then summed with the composite sync signal from the drive board to yield the CCIR-format composite video at the BNC output at the back of the camera. Timing signal I/O connections are provided at the 25-pin D connector at the back of the camera (see Pin Diagram).

Sensor scanning is controlled so that the 488 sensor line outputs are vertically centered on a correctly-adjusted 625-line monitor and the 380-elements in each line are horizontally centered across the monitor. A monitor-image exhibits a geometrically-correct image with standard 4:3 aspect ratio.

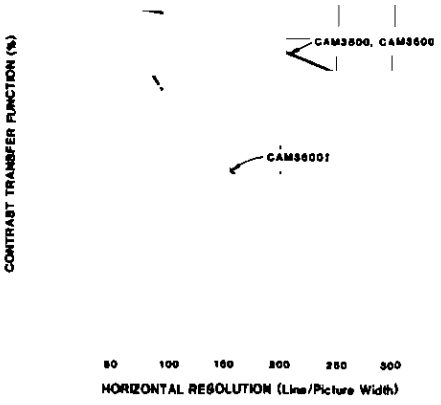
The cameras require inputs of ±15, +5 and 0.8 Amps at about +1Vdc. Internal regulators provide all voltage levels needed to drive the amplifiers and various clocks.

TYPICAL PERFORMANCE CURVES

SPECTRAL RESPONSE



CTF



* RELATIVE RESPONSE IS RELATIVE AMPLITUDE OF LOW FREQUENCY WHITE-TO-BLACK TRANSITION IN 50% WHITE SCENE

** INPUT ILLUMINATION FILTERED WITH 50-96

POWER SUPPLY

I/O PIN CONNECTIONS

HORIZONTAL DRIVE IN	COMPOSITE BLANKING OUT
HORIZONTAL DRIVE OUT	DATA RATE CLOCK OUT
VERTICAL DRIVE IN	VALID VIDEO OUT
TIMING SELECT A	+5V (500mA)
TIMING SELECT B	T.E COOLER
MASTER CLOCK+	AGC IN
MASTER CLOCK-	AGC OUT
MASTER CLOCK+ OUT	-15V (100mA) IN
MASTER CLOCK- OUT	
VERTICAL DRIVE OUT	
FIELD INDEX	
T.E COOLER	

MATING CONNECTOR IS TYPE DB-25S BY TRW OR EQUIVALENT

POWER SUPPLY UNIT

The power supply unit, which is a part of the CCD3500, CCD3600, CCD3500F, CCD3600F and CCD3500I sub-systems or which can be ordered separately for use with either of the cameras, contains a linear power supply module, timing signal buffer amplifiers and I/O signal connectors.

Power input is through a fuse-protected recessed male connector. Input voltages of 110 or 220 VAC, ±10% can be selected by an insert switch mechanism. A detachable 3-wire grounding cord with U.S. standard plug is included.

Camera Control Unit

Power Supply Cable

Power Supply Unit

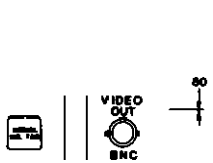
Sense Head

MECHANICAL DIMENSIONS
(NOTE ALL DIMENSIONS ARE IN INCHES)

CONTROL UNITS

SENSE HEADS

SENSE HEAD&
CONTROL UNIT
FRONT VIEWS



CONTROL UNIT
REAR VIEW
CAM3500
CAM3500F
CAM3500I

SENSE HEAD
BOTTOM VIEW
CAM3500
CAM3500F
CAM3500I

CAM3500

x The spring loaded faceplate will move inward approximately .06 inch in response to an applied force normal to the faceplate of 2 lbs.

CAM3500F

CAM3500 I

ORDER INFORMATION

CCD3500 — Includes a CAM3500 camera, remote sense head cable 12 feet (3.6 meters) in length, a power supply unit and a power supply to control unit cable. To order, specify FAIRCHILD MODEL CCD3500.

CCD3600 — Includes a CAM3600 camera, remote sense head cable 12 feet (3 6 meters) in length, a power supply unit and a power supply to control unit cable. To order, specify FAIRCHILD MODEL CCD3600.

CCD3500F — Includes a CAM3500F camera, remote sense head cable 12 feet (3.6 meters) in length, a power supply unit and a power supply to control unit cable. To order, specify FAIRCHILD MODEL CCD3500F.

CCD3600F — Includes a CAM3600F camera, remote sense head cable 12 feet (3.6 meters) in length, a power supply unit and a power supply to control unit cable. To order, specify FAIRCHILD MODEL CCD3600F

CCD3500I — Includes a CAM3500I camera, remote sense head cable 12 feet (3.5 meters) in length, a power supply unit and a power supply to control unit cable. To order, specify FAIRCHILD MODEL CCD3500I.

CAM3500 — CCIR Format camera only. To order, specify FAIRCHILD MODEL CAM3500.

CAM3600 — CCIR Format camera only To order, specify FAIRCHILD MODEL CAM3600.

CAM3500F — CCIR Format camera only with fiber optics faceplate. To order, specify FAIRCHILD MODEL CAM3500F.

CAM3600F — CCIR Format camera only with fiber optics faceplate. To order, specify FAIRCHILD MODEL CAM3600F.

CAM3500I — CCIR Format intensified CCD camera only. To order, specify FAIRCHILD MODEL CAM3500I.

Power Supply Unit — This unit provides ±15, +5 dc, and the TE cooler bias voltage inputs to the CCD3500, CAM3600, CAM3500F, CAM3600F or CAM3500I, derived from power line voltages of 110±10 or 220±20/VAC, 45–63Hz The front panel of the power supply unit provides BNC-connector access to composite blanking, composite sync, vertical drive, and horizontal drive output signals, and horizontal and vertical drive and external clock input signals plus a convenient connector for interfacing the camera and power supply to the Fairchild VIP100 Video Interface Processor.

The front panel also supports an AGC off/on switch, a clock source select switch, and a power off/on switch.

A 6' (approximately 2 meters) cable is provided for interconnection of the camera control unit and the power supply. To order, specify FAIRCHILD MODEL PWRSPLY.

Remote Sense Head Cable — Allows sense head to be remoted from camera control unit by a distance of 12' (approximately 4 meters). To order, specify MODEL CABLAUTO. Up to 4 CABLAUTOs can be used in series with little degradation in camera performance. To order, specify FAIRCHILD MODEL CABLAUTO.

Lenses — 1" Vidicon type "C"-mount lenses are available in focal lengths of 12.5mm, 25mm, and 50mm. To order, specify Models LENS12.5C, LENS25C, and LENS50C, respectively.

Monitor — CCIR monitor. To order, specify FAIRCHILD MODEL MONITOR

SPECIALS

All Fairchild Weston CCD cameras are very flexible and can be modified to suit unusual applications. Fairchild is interested in developing and manufacturing customized versions of the basic camera for volume purchasers and is willing to assist low-volume purchasers in development of custom modifications by provision of design and applications engineering assistance.

WARRANTY

Within twelve months of delivery to the end customer, Fairchild Weston CCD Imaging will repair or replace, at our option, any Fairchild Weston camera product if any part is found to be defective in materials or workmanship. Please call (408) 720-7600 in the U.S. or 081/65/618-0 in West Germany for information on assignment of a warranty return number and shipping instructions to ensure prompt repair or replacement.

CERTIFICATION

Fairchild Weston CCD Imaging certifies that this product will be carefully inspected and tested at the factory prior to shipment and will meet all requirements of the specifications under which it is furnished

FAIRCHILD WESTON

CCD IMAGING DIVISION

CAM3002/CCD3002 Solid-State Cameras and Camera Subsystems

with RS170 TIMING

FEATURES

- Buried channel CCD sensor, all solid state reliability.
- High resolution (483 × 378), high CTF (>70%).
- Element anti-blooming.
- Blemish free (see cosmetic performance specifications.)
- Small, rugged, remoteable sense head.
- Unity gamma.
- Designed for use in rugged industrial environments.
- Gen-lock capability, optional sync separator.
- Digitally controlled scanning, clock controlled frame rates.
- Selectable video AGC.
- No lag, geometric distortion, or image burn-in.
- Jumper-selectable timing/format options.
- Includes line-driven (110/220 VAC, 47-63 Hz) linear power supply plus remote sense head and power supply cables.
- Easy access to timing signal I/Os, controls.
- Complete easy to use sub-system.
- Special modifications available — consult factory.

DESCRIPTION

The CAM3002 is a rugged solid state camera designed for use in industrial environments. It is a general-purpose black and white camera incorporating RS170A standards for timing and video signals. The composite video output offers high resolution, wide dynamic range images when displayed on U.S. standard monitors or for digital analysis using RS170A-compatible image processing equipment. The camera resolution is 483 lines per frame, 378 elements per line.

CCD3002 SUBSYSTEM

CAM3002 CAMERA

The CCD3002 is a complete subsystem comprised of a CAM3002 camera, a power suppy unit which provides BNC connector access to the most often used camera I/O timing signals, a remote sense head cable, and a power supply-to-control unit cable. It is recommended that the CCD3002 subsystem be ordered for low-volume applications because of the inherent convenience of receiving an integrated camera subsystem.

The CAM3002, as pictured, can be used as a single-piece unit or separated into a camera control unit and sense head connected by a flexible cable. The sense head is designed to tolerate high accelerations, shock and vibration which might, for example, be encountered on a rapidly moving arm of an industrial robot.

Fairchild Weston Systems, Inc. CCD Imaging Division.
810 W. Maude Ave., Sunnyvale, California 94086
(408) 720-7600, TWX 910-373-2110

CAM3002 BLOCK DIAGRAM

CAM3002 SPECIFICATIONS

Scanning Format — Interlaced 2 fields per frame, 378 elements per line is standard. (Non-interlaced 1 field per frame is a pc strap option.)

Scan Timing — Frame rate is 30Hz, data rate is 7.16 elements per second under control of internal crystal-controlled oscillator. Frame rate can vary from below 5 to above 40Hz using external master clock input.

Synchronization — Can be gen-locked with horizontal and vertical drive signal inputs.

Output Signals — Analog Video: 1.4Vp-p Composite, 75 ohm, Sync (0.4Vp-p) Negative, Black =+.05V. (Sync removable with pc strap.) Timing: Vertical and Horizontal Drive, Composite Sync and Blanking, Frame Index, Data Rate Clock.

Resolution — 483 lines per picture height, 378 lines per picture width.

Sensor — Monolithic Silicon CCD. 2/3 inch vidicon format. Aspect Ratio: 4:3 (Horizontal:vertical). Image Diagonal: 11mm.

Dynamic Range — Peak signal (1V): RMS temporal noise in the dark ≥1000:1.

Saturation Irradiance — 8.4 μW/cm at normal scan rate

Minimum Illumination — S:N 20db with faceplace illumination ≥ 10^{-2} f.c.

Contrast Transfer Function, Horizontal — 75% at 378 lines/picture width.

Contrast Transfer Function, Vertical — 70% at 483 lines/picture height.

Automatic Gain Control — 10db of video gain at low light levels when activated

Cosmetic Performance (TA = 25°C, AGC OFF) — Photo response shading non-uniformity ≤5% of V_{OUT} (Video Output).

Shading in the dark ≤10mVp-p =1% max of peak output.

No sensor elements will exhibit a spurious response of ≥50 mVp-p in comparison to their nearest neighbors.

Note that the amplitude of dark signal shading non-uniformity and the amplitude of spurious non-uniformity element outputs should be expected to double for each 5 to 10°C increase in sense head temperature

Lens — C-mount standard 1" Vidicon types are recommended (See options.) Effective back focal length is 17.5mm, clear thread depth is >.25 inches.

Enclosure — Sense head is O-ring protected, thermally efficient anodized aluminum extrusion.

Weight — Sense Head, 7 oz : Sense Head and Control Unit, 2 lbs.

Environmental Conditions —
Operating Ambient Temperature: 0-50°C
Acceleration and Shock: Resistant to more than 100G, any axis
Vibration: 20-2000Hz, 20G, any axis.

Power Requirements — <8W input, ±15, +5Vdc.

INTERFACE CONNECTOR

CCD3002 SPECIFICATIONS

CAM3002 — As specified above.

Power Supply Unit — Dimensions — 7 7" wide, 4.2" high, 5.0" deep. Power Main Input — Switchable for 110 or 220 VAC, ±10% 47-63Hz, fuse protected.

Controls — Power (on/off), AGC control (on/off), Master Clock select (internal/external/gen lock).

Timing Output Signals — BNC connectors — TTL levels, horizontal drive, vertical drive, composite sync, field index.

Timing Input Signals — BNC connectors Horizontal and vertical drive for gen lock; Negative edge function, pulse amplitudes >2 Vp-p, ≤20Vdc Master clock: TTL level square wave.

9-pin D Connector — Fairchild VIP100 processor interface.

CABLAUTO 3002 — Flexible remote sense head cable, 12' (3 6 meters) long, shielded 15-pin connectors.

Power Supply Cable —Flexible power supply to camera control unit cable, 6' (1.8 meters) long, shielded 25-pin connectors.

FUNCTIONAL DESCRIPTIONS

The functional components of CCD3002 subsystems and CAM3002 cameras are illustrated in the two block diagrams as seen previously.

Image Sensor:
The image detector used in the CAM3002 camera sense head (See CAM3002 Block Diagram) is a monolithic charge-coupled device (CCD) image sensor. This sensor provides a resolution of 483 lines by 378 elements at the camera output. The buried channel CCD architecture employed in the sensor minimizes noise and allows high frame rates without sacrificing charge transfer efficiency. CCD technology allows the camera to offer zero lag and geometric distortion, lower power consumption, small size, and unusual robustness for use in industrial environments.

Sense Head:
The sense head contains the image sensor, circuitry for generating the high frequency horizontal register clock signals for CCD control, and a buffer for the sensor video. All other CCD timing and drive electronics, supply and bias voltage regulators, and video processing electonics are contained in the camera control unit. Light reaching the sensor is filtered by a 2.0mm thick Schott BG-38 glass in order to eliminate IR content and give a near photopic spectral senstivity. The sensor is rigidly held in position and aligned with respect to the sense head mounting foot. The sense head is protected by O-rings and by bonding of the filter glass into the lens mount.

Camera Control Unit:
The ca
functic
and vi
boards
master
freque
loop c
externa
compo
drive s
frame s

Timing
formati
master
board
level si
board,
to the s
to the v

The video processor receives sensor video from the CCD in the sense head. The video is line clamped, amplified, and blanked with composite blanking from the logic board, and then summed with the composite sync signal from the drive board to yield the RS170A composite video at the BNC output at the back of the camera. Timing signal I/O connections are provided at the 25-pin D connector at the back of the camera (See Pin diagram, Page 4).

The cameras require inputs of ±15 and +5Vdc Internal regulators provide all voltage levels needed to drive the amplifiers and various clocks

Power Supply Unit:
The power supply unit, which is a part of the CCD3002 subsystem or which can be ordered separately for use with a CAM3002, contains a linear power supply module, timing signal buffer amplifiers, I/O signal and interface connectors.

Power input is through a fuse-protected recessed male connector. Input voltages of 110 or 220 VAC, ±10% can be selected by an insert switch mechanism. A detachable 3-wire grounding cord with U.S standard plug is included.

CAM 3002
I/O PIN CONNECTIONS

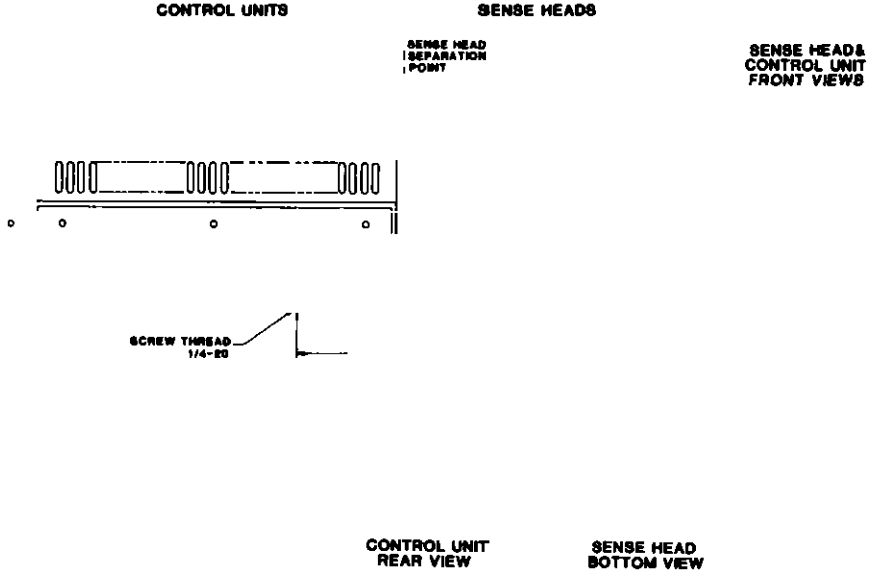
GND	
HORIZONTAL DRIVE IN	
HORIZONTAL DRIVE OUT	COMPOSITE BLANKING OUT
VERTICAL DRIVE IN	DATA RATE CLOCK OUT
TIMING SELECT A	VALID VIDEO OUT
TIMING SELECT B	
MASTER CLOCK+ IN	TRANSFER CONTROL IN
MASTER CLOCK- IN	AGC IN
MASTER CLOCK+ OUT	AGC OUT
MASTER CLOCK- OUT	-15V (100mA) IN
VERTICAL DRIVE OUT	
FIELD INDEX	
NOT CONNECTED	

MATING CONNECTOR IS TYPE DB-25S BY TRW OR EQUIVALENT

NORMALIZED RESPONSE (%)

NORMALIZED SPATIAL FREQUENCY (1.0 = 483 lines/picture HEIGHT)

CAM3002
MECHANICAL DIMENSIONS
(Note: All dimensions are in inches)



OPTIONS AND ORDER INFORMATION:

CCD3002 — Includes camera, power supply unit, remote sense head cable, and power supply cable.

CAM3002 — CCD3002 less power supply unit and cables.

Power Supply Unit — This unit provides ±15 and +5Vdc bias voltage inputs to the CCD3002 derived from power line voltage of 120±10 or 240±20 Vac, 47-63Hz. The front panel of the power supply unit provides BNC-connector access to composite blanking, composite sync, vertical drive, and horizontal drive input, output signals, an external clock input as TTL levels and connectors for interfacing the camera and power supply to the VIP100 Video Interface Processor. A 6' (approximately 2 meters) cable is provided for interconnection of the camera control unit and the power supply. To order, specify Model PWRSPLY.

Remote Sense Head Cable — Allows sense head to be remoted from camera control unit by a distance of 12' (approximately 4 meters). To order, specify Model CABL3002. Up to 4 CABL3002s can be used in series with little degradation in camera performance. To order, specify Model CABL3002.

Lenses — 1" Vidicon type "C"-mount lenses are available in focal lengths of 12.5mm, 25mm and 50mm. To order, specify Models LENS13C, LENS25C and LENS50C, respectively.

Monitor — NTSC monitor. To order, specify Model MONITOR.

WARRANTY:

Within twelve months of delivery to the end customer, Fairchild Weston CCD Imaging will repair or replace, at our option, any Fairchild Weston camera product if any part is found to be defective in materials or workmanship. Please call (408) 720-7600 for information on assignment of a warranty return number and shipping instructions to ensure prompt repair or replacement.

CERTIFICATION:

Fairchild Weston CCD Imaging certifies that this product will be carefully inspected and tested at the factory prior to shipment and will meet all requirements of the specification under which it is furnished.

All Fairchild Weston CCD cameras are very flexible and can be modified to suit unusual applications. Fairchild is interested in developing and manufacturing customized versions of the basic camera for volume purchasers and is willing to assist low-volume purchasers in development of custom modifications by provision of design and applications *engineering assistance*

FAIRCHILD WESTON

CCD IMAGING DIVISION

CAM3502/CCD3502 Solid-State Cameras and Camera Subsystems

with CCIR TIMING

FEATURES

- Buried channel CCD sensor, all solid state reliability.
- High resolution (491 × 384) high CTF (>70%).
- Element anti-blooming.
- Blemish free (see cosmetic performance specifications.)
- Small, rugged, remotable sense head.
- Unity gamma.
- Designed for use in rugged industrial environments.
- Gen-lock capability, optional sync separator.
- Digitally controlled scanning, clock controlled frame rates.
- Selectable video AGC.
- No lag, geometric distortion, or image burn-in.
- Jumper-selectable timing/format options.
- Includes line-driven (110/220 VAC, 47-63 Hz) linear power supply plus remote sense head and power supply cables.
- Easy access to timing signal I/Os, controls.
- Complete easy to use sub-system.
- Special modification available—consult factory

DESCRIPTION

The CAM3502 is a rugged solid-state camera designed for use in industrial environments. It is a general-purpose black-and-white camera incorporating CCIR standards for timing and video signals. The composite video output offers high resolution, wide dynamic range images when displayed on U.S. standard monitors or for digital analysis using CCIR compatible image processing equipment. The camera resolution is 491 lines per frame, 384 elements per line.

CCD3502 SUBSYSTEM

CAM3502 CAMERA

The CCD3502 is a complete subsystem comprised of a CAM3502 camera, a power supply unit which provides BNC connector access to the most often used camera I/O timing signals, a remote sense head cable, and a power supply-to-control unit cable.

The CAM3502, as pictured, can be used as a single-piece unit or separated into a camera control unit and sense head connected by a flexible cable. The sense head is designed to tolerate high accelerations, shock and vibration which might, for example, be encountered on a rapidly moving arm of an industrial robot.

Fairchild Weston Systems, Inc. CCD Imaging Division.
810 W. Maude Ave., Sunnyvale, California 94086
(408) 720-7600, TWX 910-373-2110

CAM/CCD3502 BLOCK DIAGRAM

CAM3500 SPECIFICATIONS

Scanning Format—Interlaced 2 fields per frame, 384 elements per line is standard. (Non-interlaced 1 field per frame is a pc strap option).

Scan Timing—Frame rate is 25Hz, data rate is 8.97M elements per second under control of internal crystal-controlled oscillator. Frame rate can vary from below 5 to above 40Hz using external master clock input. Image is displayed in center of normally-adjusted CCIR monitor.

Synchronization—Can be gen-locked with horizontal and vertical drive signal inputs.

Output Signals—Analog Video: 1.4Vp-p Composite, 75 ohm, Sync (0.4Vp-p) Negative, Black = +.05V. (Sync removable with pc strap.) Timing: Vertical and Horizontal Drive, Composite Sync and Blanking, Frame Index, Data Rate Clock.

Resolution—491 lines per picture height, 384 lines per picture width.

Sensor—Monolitic Silicon CCD. 2/3 inch vidicon format. Aspect Ratio: 4:3 (Horizontal:vertical). Image Diagonal: 11mm.

Dynamic Range—Peak signal (1V): RMS temporal noise in the dark ≥ 1000:1.

Saturation Irradiance—8.4μW/cm at normal scan rate.

Minimum Illumination—S:N 20db with faceplate illumination $\geq 10^{-2}$ f.c.

Contrast Transfer Function, Horizontal—75% at 384 lines/picture width.

Contrast Transfer Function, Vertical—70% at 491 lines/picture height.

Automatic Gain Control—10db of video gain at low light levels when activated.

Cosmetic Performance (TA = 25° C, AGC OFF)—
Photo response shading non-uniformity ≤5% of V_{OUT} (Video output).

Shading in the dark ≤ 10m Vp-p=1% max of peak output.

No sensor elements will exhibit a spurious response of ≥50 mVp-p in comparison to their nearest neighbors.

Note that the amplitude of dark signal shading non-uniformity and the amplitude of spurious non-uniformity element outputs should be expected to double for each 5 to 10° C increase in sense head temperature.

Lens—C-mount standard 1" Vidicon types are recommended. (See options.) Effective back focal length is 17.5mm, clear thread depth is > .25 inches.

Enclosure—Sense head is O-ring protected, thermally efficient anodized aluminum extrusion.

Dimensions—See figure.

Weight-Sense Head, 7 oz.; Sense Head and Control Unit, 2 lbs.

Environmental Conditions—
Operating Ambient Temperature: 0-50° C.
Acceleration and Shock:
Resistant to more than 100G, any axis.
Vibration: 20-2000Hz, 20G, any axis.

Power Requirements—<8W input, ±15, +5Vdc.

CAM3502 SPECIFICATIONS

CAM3502—As specified above.

Power Supply Unit—Dimensions—7.7" wide, 4.2" high, 5.0" deep. Power Main Input—Switchable for 110 or 220 VAC, ±10% 47-63Hz, fuse protected.

Controls—Power (on/off), AGC control (on/off), Master Clock select (internal/external/gen lock).

Timing Output Signals—BNC connectors—TTL levels, horizontal drive, vertical drive, composite sync, field index.

Timing Input Signals—BNC connectors horizontal drive, vertical drive for gen lock: Negative edge function, pulse amplitudes > Vp-p, ≤ 20Vdc. Master clock: TTL level square wave.

9-pin D Connector—Fairchild VIP100 processor interface.

CABL3502—Flexible remote sense head cable, 12' (3.6 meters) long, shielded 15-pin connectors.

Power Supply Cable—Flexible power supply to camera control unit cable, 8' (1.8 meters) long, shielded 25-pin connectors.

FUNCTIONAL DESCRIPTIONS

The functional components of CCD3502 subsystems and CAM 3502 cameras are illustrated in the two block diagrams as seen previously.

Image Sensor:
The image detector used in the CAM3502 camera sense head (See CAM3502 Block Diagram) is a monolithic charge-coupled device (CCD) image sensor. This sensor provides a resolution of 491 lines by 384 elements at the camera output. The buried channel CCD architecture employed in the sensor minimizes noise and allows high frame rates without sacrificing charge transfer efficiency. CCD technology allows the camera to offer zero lag and geometric distortion, lower power consumption, small size, and unusual robustness for use in industrial environments.

Sense Head:
The sense head contains the image sensor, circuitry for generating the high frequency horizontal register clock signals for CCD control, and a buffer for the sensor video. All

Camera Control Unit:
The camera control unit houses three pc cards, performing the functions of camera and sensor timing control, CCD drive and video processing, interconnected by two pc mother boards. Camera timing is controlled by an internal 17.94MHz master clock oscillator located on the drive board. The frequency of this oscillator is controlled by a phase locked loop circuit when the camera timing is "gen-locked" to external vertical and horizontal drive or composite video or composite sync inputs. The vertical drive input or a vertical drive separated from composite inputs is required to establish frame sync.

Timing waveforms for sensor drive and sync signals for the formation of CCIR composite video are derived from the master clock signal. These signals are then fed to the drive board when the TTL level signals are altered to CCD drive level signals required to operate the sensor. From the drive board, sensor clocks are fed through the 15-pin D connector to the sense head and the composite sync signal is forwarded to the video processor board.

The video processor receives sensor video from the CCD in the sense head. The video is line clamped, amplified, and blanked with composite blanking from the logic board, and then summed with the composite sync signal from the drive board to yield the CCIR composite video at the BNC output at the back of the camera. Timing signal I/O connections are provided at the 25-pin D connector at the back of the camera (See Pin Connectors Below).

The cameras require inputs of ±15 and +5Vdc. Internal regulators provide all voltage levels needed to drive the amplifiers and various clocks.

Power Supply Unit:
The power supply unit, which is part of the CCD3502 subsystem or which can be ordered separately for use with a CAM3502, contains a linear power supply module, timing signal buffer amplifiers, I/O signal connectors and interface connector.

Power input is through a fuse-protected recessed male connector. Input voltages of 110 or 220 VAC, ±10% can be selected by an insert switch mechanism. A detachable 3-wire grounding cord with U.S. standard plug is included.

GND
HORIZONTAL DRIVE IN
HORIZONTAL DRIVE OUT
VERTICAL DRIVE IN
TIMING SELECT A
TIMING SELECT B
MASTER CLOCK+ IN
MASTER CLOCK- IN
MASTER CLOCK+ OUT
MASTER CLOCK- OUT
VERTICAL DRIVE OUT
FIELD INDEX

TYPICAL PERFORMANCE CURVES

NORMALIZED SPECTRAL RESPONSE

NORMALIZED RESPONSE (%)

WAVELENGTH (nm)

NORMALIZED SPATIAL FREQUENCY
(1.0 = 483 lines/picture HEIGHT)

FI

VD

COMPOSITE VIDEO

FI : FIELD INDEX
MC : MASTER CLOCK

NORMAL RATE

6. VIDEO DATA RATE = $f_{MC}/8$ = 6MHz

MECHANICAL DIMENSIONS

(Note: All dimensions are in inches)

CONTROL UNITS

SENSE HEADS

SENSE HEADS
CONTROL UNIT
FRONT VIEWS

CONTROL UNIT
REAR VIEW

SENSE HEAD
BOTTOM VIEW

OPTIONS AND ORDER INFORMATION:

CCD3502—Includes camera, power supply unit, remote sense head cable, and power supply cable.

CAM3502—CCD3502 less power supply unit and cables.

Power Supply Unit—This unit provides ±15 and +5Vdc bias voltage inputs to the CCD3502 derived from power line voltage of 120±10 or 240±20 Vac, 47-63Hz. The front panel of the power supply unit provides BNC-connector access to composite blanking, composite sync, vertical drive, and horizontal drive input, output signals, an external clock input as TTL levels and connectors for interfacing the camera and power supply to the VIP100 Video Interface Processor A 6' (approximately 2 meters) cable is provided for interconnection of the camera control unit and the power supply. To order, specify Model PWRSPLY.

Remote Sense Head Cable—Allows sense head to be remoted from camera control unit by a distance of 12' (approximately 4 meters). To order, specify Model CABL3002. Up to 4 CABL3002s can be used in series with little degradation in camera performance. To order, specify Model CABL3002.

Lenses—1" Vidicon type "C"-mount lenses are available in focal lengths of 12.5mm, 25mm and 50mm. To order, specify Models LENS12.5C, LENS25C and LENS50C, respectively.

SPECIALS

All Fairchild Weston CCD cameras are very flexible and can be modified to suit unusual applications. Fairchild is interested in developing and manufacturing customized versions of the basic camera for volume purchasers, and is willing to assist low-volume purchasers in development of custom modifications by provision of design and applications engineering assistance.

WARRANTY

CERTIFICATION

Fairchild Weston CCD Imaging certifies that this product will be carefully inspected and tested at the factory prior to shipment and will meet all requirements of the specifications under which it is furnished.

FAIRCHILD WESTON

CCD IMAGING DIVISION

CAM/CCD5000 Series Solid-State Cameras and Camera Subsystems

CCD/CAM5000 SERIES FEATURES

- **Multiple camera system capability:**
  - **Cost effectiveness**
  - **Precise synchronization**
  - **Independent composite video outputs**
  - **Field expandable**
- **Very small sealed sense heads, with encapsulated circuitry, light weight and rugged.**
- **Buried channel CCD sensor, solid-state reliability, geometrically precise.**
- **Sensor is thermo-electrically cooled.**
- **RS170A format.**
- **Gen-lock and clock input capabilities for external timing control.**
- **Selectable timing/scan format options.**
- **Extended exposure for low-light-levels.**
- **Selectable video AGC.**
- **Special modifications available — consult factory.**

DESCRIPTIONS

The FAIRCHILD WESTON CAM/CCD5000 series is a family of general-purpose industrial-grade black and white solid-state RS170A-format television camera systems offering excellent electro-optical performance, versatility in timing and image scanning format and featuring very small camera sense heads for image detection. The systems are comprised of a control unit, a cable set, and one or more sense heads. The capability for operation of up to four sense heads from a single controller offers important performance and economic benefits for many applications.

Models CCD5000-1, CCD5000-2, CCD5000-3 and CCD5000-4, respectively, are complete line-powered systems including, respectively, 1, 2, 3, or 4 sense heads and correspondingly-equipped controllers. Models CAM5000-1, CAM5000-2, CAM5000-3 and CAM5000-4, respectively, include 1, 2, 3, or 4 sense heads and a controller prepared for input of dc operating voltages from customer-supplied power sources. Model CAM5000-K is a kit comprised of a sense head, cable, and a controller module to permit field additions of additional sense heads to systems.

A CCD5000 or CAM5000 camera system will provide an independent 0-1 Vp-p dc-coupled 75 ohm source impedance composite analog video output signal for each attached sense head. Video output signals comply with the RS170A specifications for 525-line, 30Hz frame rate, television systems when the camera timing is being controlled by its internal crystal

CAM/CCD5000

Fairchild Weston Systems, Inc. CCD Imaging Division
810 W. Maude Ave., Sunnyvale, California 94086
(408) 720-7600. TWX 910-373-2110

oscillator. The camera system can be synchronized with horizontal and vertical drive inputs when needed for a system application, or driven by an input clock signal for variable frame rate operation. Jumpers allow the cameras scanning formats to be changed from normal interlaced frame integration modes to non-interlaced or pseudo-interlaced field integration modes. A customer-supplied input clock can be used to increase the exposure time in frame interval increments for low-light-level image detection.

Multiple sense head self-contained Models CCD5000-2, CCD5000-3, CCD5000-4, and Models CAM5000-2, CAM 5000-3 and CAM5000-4, which do not contain the power supply module in the controller, are recommended for those applications requiring the installation of more than one RS170A format camera in a system. Sharing of functional controller modules makes the multiple camera systems cost-effective, and provides the often important performance benefits resulting from precise pixel-to-pixel synchronization of camera exposure intervals and output data scanning. Precisely synchronized scanning, for example, is critical in many stereo vision systems for 3-D inspection and other industrial applications. Multiple camera systems are also used for school bus and other large-vehicle safety installations and for security surveillance applications

Each small light-weight sense head contains a carefully selected thermo-electrically cooled 488 x 380 element buried channel charge coupled device (CCD) image sensor manufactured by Fairchild's advanced technology CCD process, plus a small circuit module providing CCD control and cable-interfacing electronics. The circuit module employs surface mounted device construction technology to achieve small size, reliability, and good high-frequency performance. The module is encapsulated into the thermally efficient sense head enclosure for ruggedness, and the optical path within the sense head is sealed by O-ring supports holding a glass filter element The sense head is designed to use industry-standard C-mount optics, and both tripod and precise dovetail camera mounting capabilities are provided on the enclosure for ease in sense head installation and positioning.

CAM5000 SENSE HEAD

The controller for a CCD5000 camera system contains an efficient line driven power supply module. The controller for a CAM5000 camera system is equipped with a connector for input of dc power from customer-supplied sources. Controllers also contain electronic modules providing the signals required for operation of the attached sense head or heads and numerous timing signal inputs and outputs which provide scan rate and format flexibility and make it easy to incorporate the camera system into machine vision applications.

Model CCD5000-1 is a self-contained one sense head system recommended for those applications using a single RS170A-format camera, the Model CAM5000-1 is a similar system using customer-supplied power supply voltage inputs into the controller. Typical examples of single-camera system applications include situations where the miniature sense head is mounted on a microscope and a monitor is used as an operator vision aid in the scientific, medical, and semiconductor communities, for harsh environment surveillance, and for image data input into machine vision hardware for robot guidance, automatic inspection, and process control in factory environments.

SERIES 5000 CONTROL UNIT

REAR

FRONT

Sensor-cooled monolithic silicon CCD.

Sensor Geometry — 1 inch vidicon format, 4:3 aspect ratio, 14.4mm image diagonal.

Scanning formats/exposure interval
Normal, 483 interlaced lines/frame, 378 elements/line, frame interval exposure.

Jumper-selectable option 1, non-interlaced 242 lines/field, field interval exposure.

Jumper-selectable option 2, pseudo-interlaced 483 lines/frame (approx. 360 lines vertical resolution), field interval exposure.

Clock controlled option, exposure interval increased in frame interval increments.

Scan timing
Normal internal control, 30Hz frame rate per RS170A specification, 7.16MHz data rate.

Gen-locked, synchronized with horizontal and vertical drive inputs.

External clock control, frame rate can be adjusted from below 1 to above 60Hz.

Note: Selection of clock source is determined by a front panel switch.

Output signals
Analog video: Independent output for each attached sense head, 1.4 Vp-p composite, sync negative, white positive, dc-coupled, 75 ohms, BNC connectors.

Timing: TTL-level vertical and horizontal drives, composite sync and blanking, odd-field index, data rate clock. Differential master clock.

Input signals (not required for normal operation)
Differential master clock for variable frame rate.

Horizontal and vertical drives for gen-locking: TTL Levels.

Resolution — >50% CTF at 483 lines per picture height (in full-interlaced mode), 378 lines per picture width.

Sensitivity — >20db S/N with faceplate illumination $\geq 10^{-2}$ footcandles.

I/O PIN CONN

VIP/AUX CONNECTOR **CAMERA I/O CO**

DIGITAL GND	DIGITAL GND
N/C	RESET
N/C	N/C
N/C	N/C
N/C	N/C
N/C	TRANSFER CONTROL
HD OUT	VD OUT
CB OUT	VALID VIDEO
HD IN	VD IN
MC+ OUT	MC-OUT
MC+ IN	MC- IN
DIGITAL GND	FL
	DRC

CCD5000 MECHANICAL DIMENSIONS

(NOTE: ALL DIMENSIONS ARE IN INCHES UNLESS SPECIFIED)

CONTROL UNIT

CABL5000

SENSE HEAD

SIDE VIEW

FRONT VIEW

'C' MOUNT
LENS THREAD
1.00-32

1/4-20
MOUNTING HOLE

SYSTEM CONFIGURATIONS

A Model CAM5000-1 is the same as a Model CCD5000-1, except that the controller is equipped with a connector for dc power inputs, and does not contain the line-driven power supply module.

Self-contained two, three or four sense head systems are ordered by specifying Models CCD5000-2, CCD5000-3, or CCD5000-4, respectively. The controller for the multiple camera systems is equipped with one additional camera control board for each additional sense head ordered. Only one power module and one timing module are used in the multiple camera systems. Models CAM5000-2, CAM5000-3, and CAM5000-4 are 2, 3, and 4 sense head systems, respectively, not equipped with the power module in the controller.

FUNCTIONAL COMPONENTS

IMAGE SENSOR

The image sensor employed in the CCD/CAM5000-series

THERMO-ELECTRIC COOLER

OPTICS

SENSE HEAD CIRCUITRY

SENSE HEAD ENCLOSURE

CONTROLLER

POWER SUPPLY MODULE

The power supply module is a low-noise switching circuit which accepts 110 or 220 VAC, ±10% 47–440Hz inputs. Inputs are fuse protected with chassis grounding. All outputs of the module are regulated and well-filtered.

TIMING CONTROL MODULE

Camera system timing is normally controlled by an internal 14.3MHz Master Clock oscillator Timing signals for sensor drive and synchronizing signals for formation of RS170A composite video are derived from the Master Clock signals. The frequency of a second internal voltage-controlled Master Clock oscillator is determined by a phase-locked-loop circuit which compares the phase of the internally-generated and external horizontal drive input signals when the camera is "gen-locked" to external equipment A vertical drive input signal is required to establish frame sync in the gen-lock mode. Master Clock inputs from an external signal source can be used for variable frame rate operation

CAMERA CONTROL MODULE

Special purpose amplifiers on the camera modules convert the TTL-level timing signals generated on the timing module into proper CCD drive clocks. Adjustable regulators permit sensor performance optimization. The CCD clock waveforms and adjusted bias voltages are transmitted to the sense head through the cable.

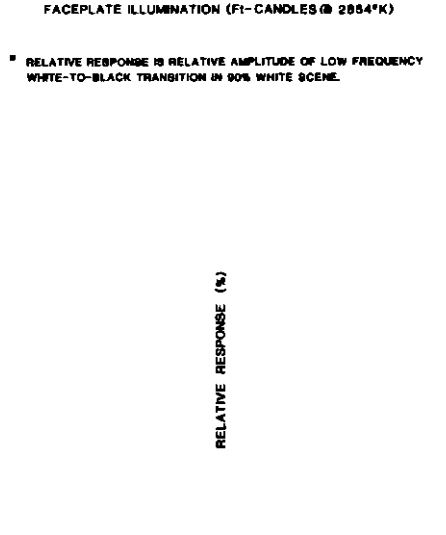
The video processing circuitry on the camera control board receives sense head video through the cable. The video is line-clamped for dc restoration, amplified, blanking is inserted, and then summed with the sync signal to yield an RS170A composite video output. Video automatic gain control amplification is switch-selectable. About 10db of additional gain is available for low light level inputs.

CABLES

Shielded cables, 12 feet in length, are provided for interconnection of the sense head on the controller. The cable diameter is about 3/8 inch. Special construction techniques and material provides a tough, flexible cable.

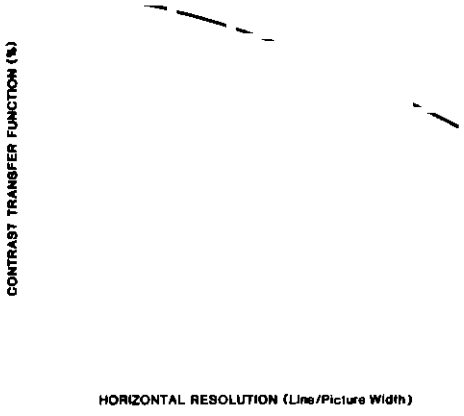
TYPICAL PERFORMANCE CURVES

TRANSFER CHARACTERISTIC



* RELATIVE RESPONSE IS RELATIVE AMPLITUDE OF LOW FREQUENCY WHITE-TO-BLACK TRANSITION IN 90% WHITE SCENE.

CTF



ORDER INFORMATION

Self-contained camera systems, including sense head or heads, controller with line driven power supply and electronic modules, cables, and operating manual. To order, specify FAIRCHILD MODEL:

CCD5000-4 for 4 sense head system
CCD5000-3 for 3 sense head system
CCD5000-2 for 2 sense head system
CCD5000-1 for 1 sense head system

Camera systems without power supply module and with dc input connector in controllers. To order, specify FAIRCHILD MODEL:

CAM5000-4 for 4 sense head system
CAM5000-3 for 3 sense head system
CAM5000-2 for 2 sense head system
CAM5000-1 for 1 sense head system

Expansion kit for field additions of sense heads to CCD5000 systems. Comprised of a sense head, camera control module, and cable. To order, specify FAIRCHILD MODEL CAM5000-K.

Lenses — 1" Vidicon type "C"-mount lenses are available in focal lengths of 12.5mm, 25mm, and 50mm. To order, specify FAIRCHILD MODELS LENS12.5C, LENS25C and LENS50C, respectively.

Monitor — Black and white monitor. To order, specify FAIRCHILD MODEL MONITOR.

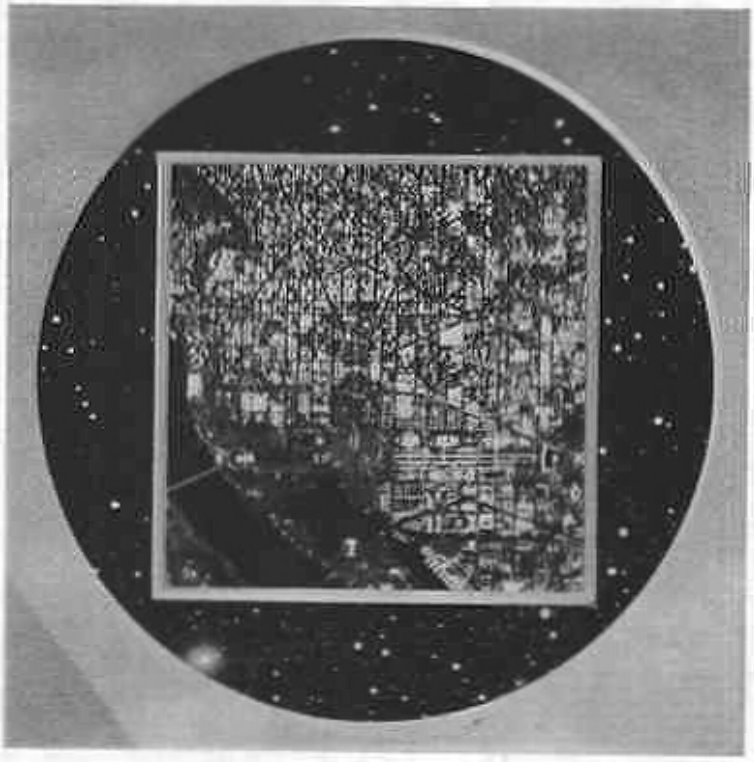
SPECIALS

WARRANTY

Within twelve months of delivery to the end customer, Fairchild Weston CCD Imaging will repair or replace, at our option, any Fairchild Weston camera product if any part is found to be defective in materials or workmanship. Please call (408) 720-7600 in the USA or 081 65/618-0 in West Germany for information on assignment of a warranty return number and shipping instructions to ensure prompt repair or replacement.

CERTIFICATION

Fairchild Weston CCD Imaging certifies that this product will be carefully inspected and tested at the factory prior to shipment and will meet all requirements of the specifications under which it is furnished.



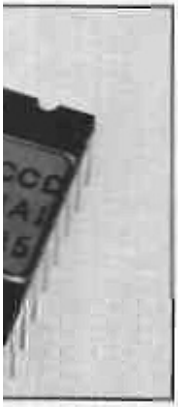
Signal Processing

Fairchild Weston CCD Imaging provides sophisticated devices and systems for inspection, measurement, surveillance, telecine, facsimile & optical character recognition, in industry, science, medicine, defense and many other fields.

FAIRCHILD WESTON

CCD IMAGING DIVISION

CCD321A/B 455/910—Bit Analog Shift Register Charge Coupled Device



FEATURES

- Electrically variable analog delay line for audio and video applications.
- 1 H video delay line capability with broadcast quality performance.
- Excellent bandwidth at video and audio rates due to buried channel technology.
- Wide range of data rate: from 10 kHz to 20 MHz per 455 section.
- High signal to noise ratio — Video: 58 dB, Audio: 65 dB.
- Special modifications available — consult factory.

DESCRIPTION

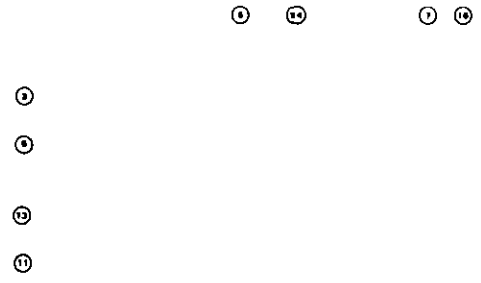
The CCD321B is an improved pin-for-pin replacement for the CCD321A. The CCD321 is available in four different classes as follows:

DEVICE	APPLICATION
CCD321A-1	Broadcast quality video delay line
CCD321A-2/B-2	Industrial video delay line
CCD321A-3/B-3	Time base compression and expansion delay line
CCD321A-4/B-4	Audio delay line

Φ_{1A},Φ_{1B}	Analog Shift Register Transport Clocks
Φ_{SA},Φ_{SB}	Input Sampling Clocks
Φ_{RA},Φ_{RB}	Output Sample and Hold Clocks
V_2	Analog Shift Register DC Transport Phase
V_{IA},V_{IB}	Analog Inputs
V_{RA} V_{RB}	Analog Reference Inputs
V_{OA},V_{OB}	Analog Outputs
V_{DD}	Output Drain
V_{GG}	Signal Ground
V_{SS}	Substrate Ground

Fairchild Weston Systems, Inc. CCD Imaging Division
810 W. Maude Ave., Sunnyvale, California 94086
(408) 720-7600, TWX 910-373-2110

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION — The CCD321 consists of the following elements illustrated in the Block Diagram:

Two Charge Injection Ports — The analog information in voltage form is applied to two input ports at V_{IA} (or V_{IB}). Upon the activation of the analog sample clocks ϕ_{SA} (or ϕ_{SB}) a charge packet linearly dependent on the voltage difference between V_{IA} and V_{RA} (or V_{IB} and V_{RB}) is injected into analog shift register A (or B).

Two 455-Bit Analog Shift Registers — Each register transports the charge packets from the charge injection port to its corresponding output amplifier. Both registers are operated in the 1-1/2 phase mode where one phase (ϕ_{1A} or ϕ_{1B}) is a clock and the other phase (V_2) is an intermediate dc potential. Phases ϕ_{1A} and ϕ_{1B} are completely independent. V_2 is a dc voltage common to both registers.

Two Output Amplifiers — Charge packets from each analog shift register are delivered to their corresponding output amplifier as shown in the circuit diagram. Each output amplifier consists of three source follower stages with constant current source bias. A sample and hold transistor is located between the second and third stage of the amplifier. When the gate of the sample and hold transistor is clocked (ϕ_{RA} or ϕ_{RA}) a continuous output waveform is obtained as shown in the timing diagrams. The sample and hold transistor can be defeated by connecting ϕ_{RA} and/or ϕ_{RB} to V_{DD}. In this case the output is a pulse modulated waveform as shown in the timing diagram.

MODES OF OPERATION — The CCD321 can be operated in four different modes:

455-Bit Analog Delay — Either 455-bit analog shift register can be operated independently as a 455-bit delay line. The driving waveforms to operate shift register A is shown in Fig. 10. The input voltage signal is applied directly to V_{IA}. The input sampling clock ϕ_{SA} samples this input voltage and injects a proportional amount of charge packet into the first bit of register A. The input voltage A_1 which is sampled between $t = 0$ and $t = t_C$ appears at the output terminal V_{OA} @ $t = 910t_C$. If the sample and hold circuit is not used then the output appears as a pulse amplitude modulated waveform as shown in the diagram. In that case ϕ_{RA} (pin 7) should be connected to V_{DD} (pin 16). If the sample and hold circuit is used then the output appears as a continuous waveform. Here ϕ_{RA} (pin 7) should be clocked coincident with ϕ_{SA} (pin 5) and the two pins can be connected together.

Analog shift register B can be operated in an analogous manner with V_{IB} as the analog input, ϕ_{1B} as the transport clock, ϕ_{SB} as the input sampling clock and ϕ_{RB} as the output sample and hold clock.

910-Bit Analog Delay in Series Mode — The two analog shift registers A and B can be connected in series to provide 910 bits of analog delay as shown in the schematic below. The analog signal input voltage is applied to V_{IA}. The output of register A is connected to the input of register B with a simple emitter follower buffer stage. In order to insure proper charge injection of register B , V_{RB} should be adjusted. The timing diagram shown in Fig. 10 applies in this mode of operation. Here $\phi_{1A} = \phi_{1B}$, $\phi_{SA} = \phi_{SB}$, $\phi_{RA} = V_{DD}$, and ϕ_{RB} is clocked.

SIGNAL OUT

910-Bit Analog Delay in Multiplexed Mode — The two analog shift registers can be connected in parallel to provide 910-bit of analog delay as shown in the schematic below. The analog signal input voltage is applied to both V_{IA} and V_{IB}. The outputs at V_{OA} and V_{OB} can be combined as shown in Fig. 8 to recover the analog input information.

The necessary waveforms to operate the device in this mode is shown in Fig. 11. In this case ϕ_{SA} samples the analog input A_1 at V_{IA} between $t = 0$ and $t = t_C$. ϕ_{SB} samples the analog input B, at V_{IB}, between $t = t_C$ and $t = 2t_C$. The output corresponding to A_1 appears at V_{OA} at $t = 910t_C$. The output corresponding to B_1 appears at V_{OB} @ $t = 911t_C$. This mode of operation results in an effective sampling rate of twice the rate of ϕ_{1A}, ϕ_{1B}, ϕ_{SA} and ϕ_{SB}.

The CCD321 is available in four different classes for different applications. The CCD321A-1 is a high quality broadcast 1H delay line for video systems with 1% differential gain and 1° differential phase. The CCD321A-2/B-2 is a high quality video delay line with 3% differential gain and 3° differential phase.

The CCD321A-3/B-3 is tested in the START/STOP mode of operation and parameters are guaranteed in this mode. The CCD321A-4/B-4 is tested at audio speeds; audio parameters are specified and guaranteed. The dc and clock characteristics of the four classes are the same. The ac characteristics vary as shown below.

Caution: The device has limited built-in gate protection. Charge build-up should be minimized. Care should be taken to avoid shortings pins V_{OA} and V_{OB} to ground during operation of the device.

DC CHARACTERISTICS: T_A = 55°C, Note 16

Shift Register DC Transport

R_{IN}	Small Signal Input Resistance		1.0	MΩ	Resistance from Pins 3, 4, 12 or 13 to V_{SS}. V_{IA} = V_{IB} = 3 V
C_{IN}	Small Signal Input Capacitance		10	pF	Capacitance from Pins 3, 4, 12 or 13 to V_{SS}. V_{IA} = V_{IB} = 3 V

Output DC Mismatch Between A & B Registers

Output AC Mismatch Between A & B Registers

CLOCK CHARACTERISTICS: T_A = 55°C, Note 16

SYMBOL	CHARACTERISTICS	RANGE MIN	RANGE TYP	RANGE MAX	UNITS	CONDITIONS
$V\phi_{1AL}$, $V\phi_{1BL}$	Analog Shift Register Transport Clocks LOW	0	0.5	0.8	V	Note 4
$V\phi_{1AH}$, $V\phi_{1BH}$	Analog Shift Register Transport Clocks HIGH	12.0	13.0	15.0	V	Note 4
$V\phi_{SAL}$, $V\phi_{SBL}$	Input Sampling Clocks LOW	0	0.5	0.8	V	Note 5
$V\phi_{SAH}$, $V\phi_{SBH}$	Input Sampling Clocks HIGH	12.0	13.0	15.0	V	Note 5
$V\phi_{RAL}$, $V\phi_{RBL}$	Output Sample and Hold Clocks LOW	0	0.5	0.8	V	Note 6
$V\phi_{RAH}$, $V\phi_{RBH}$	Output Sample and Hold Clocks HIGH	12.0	13.0	15.0	V	Note 6
$f\phi_{1A}$,$f\phi_{1B}$	Analog Shift Register Transport Clock Frequency	0.02		20	MHz	See Note 17
$f\phi_{SA}$,$f\phi_{SB}$	Input Sampling Clocks Frequency	0.02		20	MHz	See Note 17
$f\phi_{RA}$,$f\phi_{RB}$	Output Sample and Hold Clocks Frequency	0.02		20	MHz	See Note 17

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−25°C to 100°C
Operating Temperature	−25°C to 55°C
All Pins with Respect to V_{SS}	−0.3 V to 18 V

CCD321A-1 AC CHARACTERISTICS: T_A = 55°C Both registers in the multiplexed mode, Clock Rate = 7.16 MHz. Sampling Rate = 14.32 MHz. Vout = 700 mV. (See Test Load Configuration, Figure 8)

SYMBOL	CHARACTERISTIC	RANGE MIN	RANGE TYP	RANGE MAX	UNITS	CONDITIONS
BW	Signal Bandwidth (3 dB Down)	5.0			MHz	Note 7
IG	Insertion Gain		3.0			Note 8
Δ G	Differential Gain				%	Note 9
Δ φ						Note 9
						Note 10
$V_{I\ (max)}$					V_{pk-pk}	

Clock Rate = 7.16 MHz,

						CONDITIONS
						Note 7
						Note 8
					%	Note 9
Δ φ	Differential Phase					Note 9
						Note 10
$V_{I\ (max)}$					V_{pk-pk}	

Clock Rate = 7.16 MHz,
Configuration, Figure 8)

						CONDITIONS
						Note 7
						Note 8
					%	Note 9
Δ φ						Note 9
						Note 10
	Spacial Noise					Notes 11, 12
$V_{I\ (max)}$						

CCD321A-2/B-2 AC CHARACTERISTICS: T_A = 55°C Both registers in the multiplexed mode, Clock Rate = 7.16 MHz, Sampling Rate = 14 32 MHz. V_{OUT} = 700 mV. (See Test Load Configuration, Figure 8)

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
BW	Signal Bandwidth (3 dB Down)	23	25		kHz	Note 7
IG	Insertion Gain	0	3.0	6.0	dB	Note 8
THD					%	
S/N						
$V_{I\ (max)}$						
RSO						

±1 V mi be necessary to maximize signal bandwidth.
of either or Vs is necessary to assure proper operation.
ction from substrate to the shift registers. A negative bias on

4.
5.
6.
7.
8.
9.
10.
11.
12.
13.
14.
15.
16.
17.

DIFFERENTIAL GAIN — %
DIFFERENTIAL PHASE — DEGREES

DIFFERENTIAL GAIN — %
DIFFERENTIAL PHASE — DEGREES

SIGNAL TO NOISE RATIO -dB $\frac{\text{peak to peak}}{\text{rms}}$

Fig. 3

TYPICAL AUDIO PERFORMANCE CURVES

TOTAL HARMONIC DISTORTION (THD) AND S/N RATIO VERSUS V_{OUT}

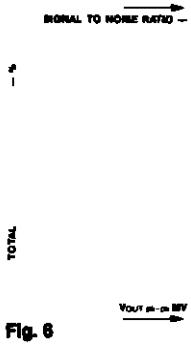


Fig. 6

RATE OF AVERAGE SIGNAL OFFSET VERSUS TEMPERATURE

TEST LOAD CONFIGURATION FOR MULTIPLEXED OPERATION IN VIDEO

TEST LOAD CONFIGURATION FOR SINGLE REGISTER OPERATION IN AUDIO AND VIDEO

TIMING DIAGRAM

NOTE:
This timing diagram also applies for shift register B. In this case ϕ_{1A} becomes ϕ_{1B}, ϕ_{SA} becomes ϕ_{SB}, V_{IA} becomes V_{IB} and V_{OA} becomes V_{OB}.

Fig. 10 Analog Shift Register A or B Operation

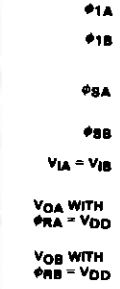


Fig. 11 Analog Shift Register A and B Operation in the Multiplexed Mode

CIRCUIT DIAGRAM

ORDERING INFORMATION

To order the CCD321 specify the "device and package type" as shown below:

CLASS, APPLICATION	SIDEBRAZE PKG.	CERDIP PKG.
Broadcast quality video	CCD321A1	
Industrial quality video	CCD321A2	CCD321B2
Time base compression and expansion	CCD321A3	CCD321B3
Audio delay line	CCD321A4	CCD321B4

Also available from Fairchild is a fully-assembled module that contains all the necessary circuitry to operate the CCD321. The module is designed to help the system designer become familiar with the operation of the device, and for use in OEM systems.

The CCD321VM is a video module using a CCD321A-3 or B-3. The module includes the necessary electronics to perform time base compression and expansion, and variable video signal delay. The module requires a single power supply for operation.

Schematics and component layouts are included in the shipping packages for the CCD321VM. For further information on the CCD321VM please contact your nearest Fairchild sales office or distributor or call 408-720-7600.

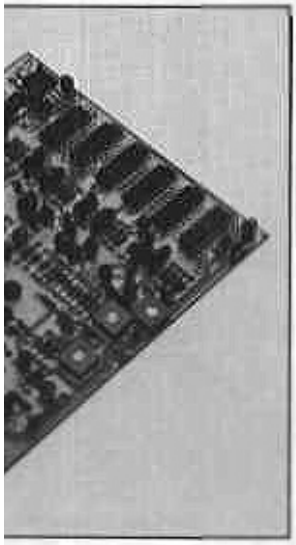
CCD321A: 16-PIN SIDEBRAZED

NOTES:
All dimensions in inches (bold) and millimeters (parentheses).
Header is black ceramic (Al_2O_3)
Pins are Alloy 42, plated with gold (321A) or nickel (321B).
Top cover connected to pin 8 (V_{SS} substrate) on 321A

FAIRCHILD WESTON

CCD IMAGING DIVISION

CCD321VM
Video Delay Module



FEATURES

- 1 H delay line performance
- Electrically variable delay
- Adjustable delay — by clock control
- Wide signal bandwidth — 5 MHz
- High S/N ratio — 55 dB
- Dual 455-bit or single 910-bit delay
- No drift — delay dependent on clock frequency
- Internal or external clocking
- Temporary storage operation controlled by a single TTL input line
- Single polarity power supply - +20 V

DESCRIPTION

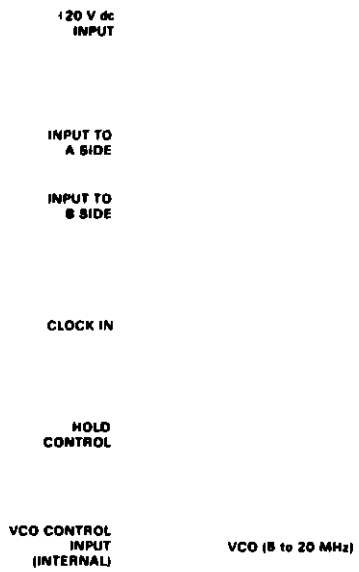
The CCD321VM is a complete delay module intended for use in

The delay time of analog signals through the CCD321VM is precisely controlled by the clock signal frequency which can be provided by an external source or obtained from an internal VCO. The CCD321VM can be used as a 910-bit one horizontal line (1H) delay for TV video bandwidths of 5 MHz when operating with a $4 \times 3.58 = 14.3$ MHz clock frequency, serve as a temporary analog store for a full-bandwidth TV line, or can be used as an adjustable delay by controlling either the internally generated or external input clock. The CCD321VM can also be used as two 455-bit registers for delay of two independent analog signals.

Typical video applications for the CCD321VM include time-based correctors, video re-synchronizing systems, comb filter realizations, moving target indicators and signal-to-noise enhancement systems. Other applications include time-based compression and expansion systems, phase delay equalizers and general purpose analog delay.

Fairchild Weston Systems, Inc. CCD Imaging Division.
810 W. Maude Ave., Sunnyvale, California 94086
(408) 720-7600, TWX 910-373-2110

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Dual 455-Bit Analog Shift Register: CCD321

The Fairchild CCD321 is a monolithic 455/910-bit charge coupled device analog shift register packaged in a 16-pin dual in-line package. Functionally this device employs discrete electronic charge packets representing the sampled amplitudes of two analog input voltage waveforms that are transported towards output charge sensing amplifiers by a 1-1/2 phase digital clock signal. An integrated sampled and hold output stage provides register output waveforms which are near-replicas of the signals input to the device 455 periods earlier. (See CCD321 Data Sheet for more details concerning this device.)

Clocking Logic and Driver Circuits — The transport and sampling clock pulses required for control of the CCD shift register are generated at TTL levels and then amplified and waveshaped by clock line drivers. A transport and a sample pulse for register A of the CCD321 is triggered by each LOW-to-HIGH transition of the master clock input to the CCD321VM; a clock pair for register B is triggered by each LOW—to—HIGH clock input transition. Analog information is thus made to travel completely through both sides of the shift register by 455 complete cycles of the input clock.

Storage Logic — A TTL HIGH level on the Enable input terminal of the CCD321VM is synchronized to the transport clock pulses and stops the transport and sampling functions of the register. The analog data in the registers when the clocks are stopped is stored until the Enable line returns LOW, and then transported out in the usual manner.

Signal Processing — Signal inputs to the A and B registers of the CCD321 are gain-controlled by individual potentiometers and then ac coupled through 22 μF capacitors into 100 K Ω loads at the device inputs. Two emitter-followers provide the sampled and held register A and register B ouput waveforms at a 75 Ω source impedance level.

If the two signal input terminals are connected together, the input data is sampled twice during each clock cycle. Alternate sampled analog bits go in sequence to the two registers of the CCD321. These alternating samples are de-multiplexed at the register output, low pass filtered, and given to a third video output lead. A 910-bit resolution is thus obtained, giving a signal delay of 455 clock periods or 910 clock half cycles. This multiplex operating mode provides 63.5 μs delay for a 5 MHz bandwidth signal using a clock input frequency of 2 × 3.58 MHz = 7.16 MHz, equivalent to a 14.3 MHz sampling and transport rate.

Clock Oscillator — The internal clock generator of the CCD321VM is a VCO which can be controlled over a 5 to 20 MHz range by an external 0 to 5 Vdc signal, or adjusted by an on-board potentiometer. An external TTL compatible square wave clock signal can also be used by optional connector wiring.

Bias Control —Power input to the CCD321VM is from a nominal +20 V extrnal supply. On-board regulators control bias voltages for the CCD321, drivers and logic circuitry.

DC CHARACTERISTICS

SYMBOL	PARAMETER	UNIT	CONDITIONS	MODULE PIN NUMBER
		+20 Vdc (<400 mA)		
			—	ins
V_{IA}				
VCO (IN)				
	Bandwidth (3 db down)			
$\Delta\phi$				
	Total Harmonic Distortion		2% Max	
			1% Max	

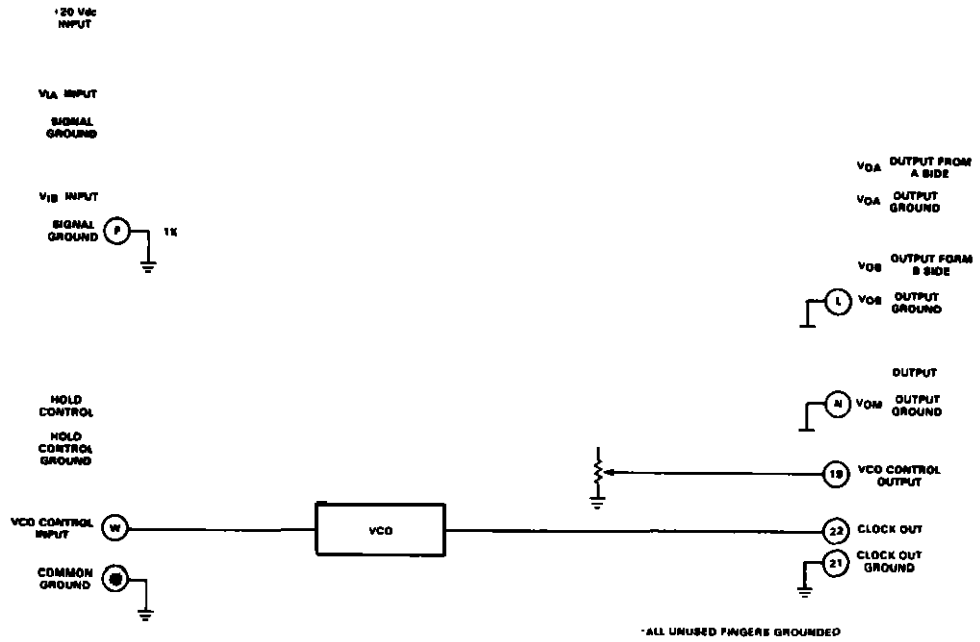
NOTES:

1. Module operates from 19 to 24 Vdc.
2. f_{IN} is the clock of a single register. In the series or independent register mode, a sampling clock of 4X the signal bandwidth is usually required. In the multiplex mode, a sampling clock of 2X the signal bandwidth is required. (I.e., in the multiplex mode of operation, with f_{IN} = 10 MHz per side a 5 MHz (3db) bandwidth can be processed through the device.)
3. AC parameters guaranteed from 0° C to 55° C. Delay tolerances determined by stability of clock frequency.
4. Measured on a Tektronics 520 VECTORSCOPE.
5. Using f_{IN} = 10 MHz, multiplexed mode, V_{IA} = V_{IB} = 500 mV peak-to-peak, 1 MHz sine wave. Measurement done using spectrum analyzer.
6. Using Rhode and Schwartz noise meter at 4.2 MHz bandwidth
7. This is a dc offset on the output signal which can occur because of dark current build-up when in hold mode. This offset can be expected to double for each 8-10° C increase in the CCD321 junction temperature.

Modes of Operation and Connection Diagrams
The CCD321VM can be operated in various modes: (1) Two independent 455-bit analog registers, (2) multiplex, (3) series and (4) temporary analog storage. An on-board generated clock with adjustable frequency, and internal VCO controlled clock or an independent externally generated clock input can be used in any of the four modes.

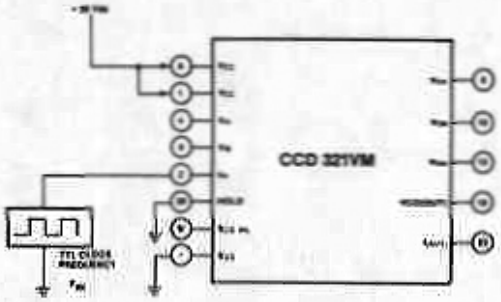
The circuit diagram shown below shows the pin nomenclature for the CCD321VM.

The following diagrams represent the correct input/output connections for proper operation of the CCD321VM in the various modes. The CCD321VM circuit diagram is included in the module shipping package.



Mode 1: Internal Clock, Adjustable Frequency (R1)

Mode 2: Internal Clock, V_{CO} Input Variable Delay



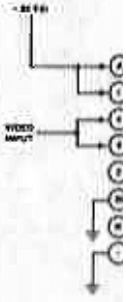
Mode 3: External Input Clock

Note 1: Delay = $\frac{455}{f_{IN}}$

Mode 4: Two Register Parallel Delay

Notes:

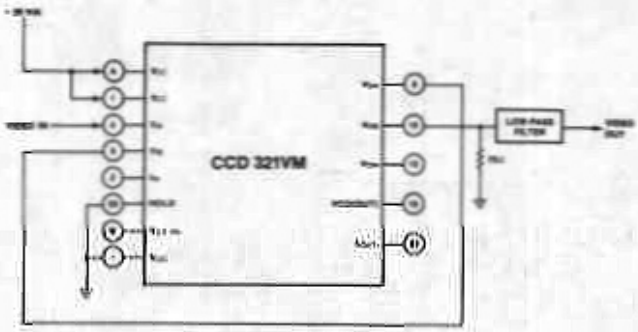
1. Depending on requirements, connect pins Z, W, 19 and 22 for internal or external clocking as shown in Modes 1, 2 and 3.
2. Delay = $\frac{455}{f_{IN}}$



Mode 5: Multiplexed Mode of Operation

Notes:

1. Depending on requirements, connect pins Z, W, 19 and 22 for internal or external clocking as shown in Modes 1, 2 and 3.
2. Delay = $\frac{455}{f_{IN}}$



Mode 6: Series Mode of Operation

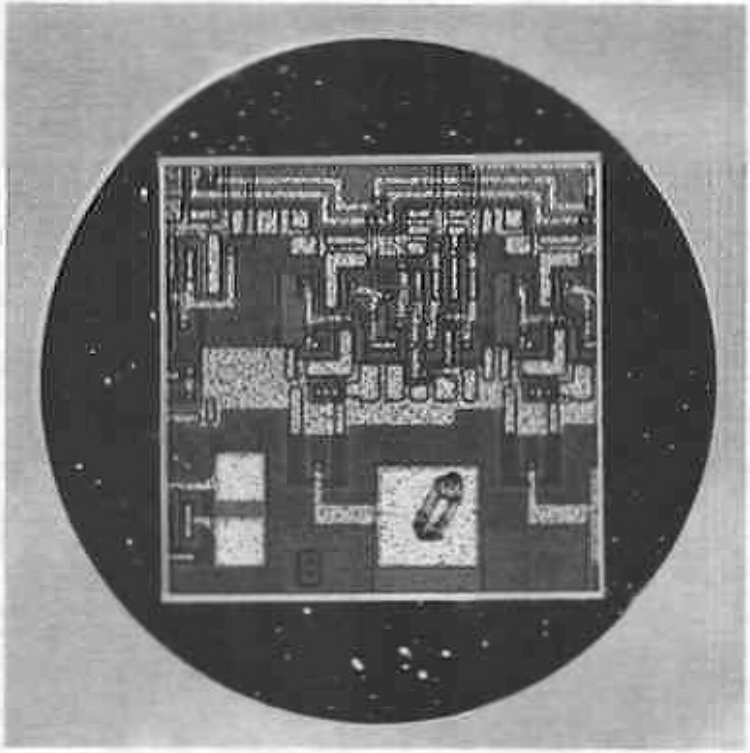
Notes:
1 Depending on requirements, connect pins Z, W, 19 and 22 for internal or external clocking as shown in Modes 1, 2 and 3.

2 Delay = $\frac{910}{f_{IN}}$

Mode 7: Temporary Analog Storage Operation

Notes:
1 Depending on requirements, connect pins Z, W, 19 and 22 for internal or external clocking as shown in Modes 1, 2 and 3.

2 Store signal (TTL)



Application Notes, Articles and Technical Briefs

Charge-Coupled Devices

The products of a new concept in semiconductor electronics, they hold considerable promise in applications as diverse as image sensors and information-storage elements for computer memories.

By Gilbert F. Amelio *Reprinted from Scientific American February 1974*

For the past four years there has been a growing excitement among solid-state physicists about a new concept in semiconductor electronics that may someday have an impact on our lives as dramatic as that of the transistor. The new concept is charge-coupling and its practical manifestation is the charge-coupled device.

Like the transistor, the charge-coupled device is a concept of semiconductor electronics; as such it is subject to the same physical laws that govern the transistor's dynamics and fabrication. That, however, is where the similarity ends. Although the charge-coupled device shares much the same technological base with its distinguished predecessor, it is a functional concept that focuses on the manipulation of information rather than an active concept that focuses on the modulation of electric currents. Transistor technology has made possible computer-memory components with thousands of memory elements on a single chip of silicon; charge-coupling is making possible comparably sized memory components with tens of thousands or even hundreds of thousands of memory cells per silicon chip at approximately the same cost.

What is charge-coupling? It is the collective transfer of all the mobile electric charge stored within a semiconductor storage element to a similar, adjacent storage element by the external manipulation of voltages. The quantity of the stored charge in this mobile "packet" can vary widely, depending on the applied voltages and on the capacitance of the storage element. The amount of electric charge in each packet can represent information.

Perhaps the easiest way to visualize the operation of a charge-coupled device is through the use of a mechanical analogy. Imagine a machine consisting of a series of three reciprocating pistons with a crankshaft and connecting rods to drive them [*see top illustration on next two pages*]. On top of one or more of the pistons is a fluid. Note that rotating the crankshaft in a clockwise manner causes the fluid to move to the right, whereas rotating the crankshaft in a counterclockwise manner would cause the fluid to move to the left. Since it takes three pistons to repeat the pattern, this arrangement is called a three-phase system. If it is desired to move the fluid in one direction only, a two-phase system can be devised by imposing an asymmetry on the piston design [*see bottom illustration on next two pages*]. Regardless of the direction of rotation, the fluid now advances to the right.

Analogous charge-coupled devices can be fabricated of silicon [*see illustrations on page 26*]. The devices consist of a "*p* type" silicon substrate (in which electrons are normally the signal carriers) with a silicon dioxide insulating layer on its surface. An array of conducting electrodes is deposited in turn on the surface of the insulator. The electrodes can be interconnected to establish either two-phase or three-phase operation. Underlying the insulator and within the bulk of the semiconductor the electrical conductivity of the silicon can be selectively altered to form "*n* type" material (in which not electrons but electron "holes" are normally the signal carriers).

The correspondence with the machine in the mechanical analogy is realized by supposing that the fluid represents an accumulation of electrons, that the pistons represent the potential energy associated with the voltages applied to the electrodes and that the crankshaft and connecting rods represent the driving voltages and their relative timing.

When a periodic wave form called a "clock" voltage is applied to the electrodes, some of the electrons in the vicinity of each electrode will form a discrete packet of charge and move one charge-coupled element, or unit cell, to the right for each full clock cycle. The packets of electron charge therefore move to the right as a result of the continuous lateral displacement of the local "potential well" in which they find themselves. They are thus—or so it seems—always falling.

The creation of the necessary potential well in the semiconductor substrate deserves some elaboration because of its central importance to the charge-coupling concept. In this context a potential well is a localized volume in the silicon that is attractive to electrons; in other words, it is the most positive place around and hence is a desirable location from the point of view of the negative electron. Potential wells are formed in a charge-coupled storage element by the interaction of the different conductivity-type regions of the silicon [*see illustration on page 27*]. This interaction forms a well for electrons such that the higher the clock voltage, the deeper the well. Any electrons in the well will move with the clock voltages.

Now, if two or more wells of different depths are placed close to one another, the wells will overlap and charge may be "coupled," or transferred, from one storage element to the next as the depth of the well is altered by the clock voltages. Thus the external clock voltages on the electrodes cause the electrons to move in packets through the semiconductor in a potential-energy trough known as a channel. This mode of electron transfer is the essence of charge-coupling.

Closeup View *of a small portion near the output of a charge-coupled photosensor array is provided by this scanning electron micrograph. Each element and its associated readout electrode measure 1.9 square mils.*

The phenomenon of charge-coupling is in itself inadequate for the purpose of constructing a useful device. A practical charge-coupled device must be able to introduce the necessary electrons into the structure and also have a means at some location in the channel for detecting the amount of charge in a packet. Thus for a structure to be classified as a charge-coupled device it must possess at least three attributes: input, charge-coupling and output.

source. The input-gate voltage is now lowered to isolate the source, and the charge packet created is ready for transfer down the channel. In the detection of the signal the charge is merely transferred to a "drain," or output diode, where it appears as a current in some external circuit. This simple charge-coupled device fulfills the function of an eight-bit shift register, a device potentially useful in computer architecture.

Mechanical Analogy *useful in visualizing the operation of a charge-coupled device is depicted in this sequence of idealized drawings. The machine illustrated consists of a repeating series of three reciprocating pistons with a crankshaft and connecting rods to drive them. On top of one or more of the pistons is a fluid (color). Rotating the crankshaft in a clockwise manner, as shown in this instance, causes the fluid to move to the right. If the crankshaft were to be rotated in a counterclockwise manner, on the other hand, the fluid would move to the left. This particular type of arrangement, which requires three pistons to repeat the pattern, is called a three-phase system. An analogous charge-coupled device can be fabricated of silicon (see top illustration on next page).*

Asymmetrical Pistons *are added to the mechanical analogue in order to introduce the operating principle of a two-phase system. Regardless of the direction in which the crankshaft is rotated, the fluid now advances to the right. In the correspondence with an actual charge-coupled device the fluid represents an accumulation of electrons, the pistons represent the potential energy associated with the applied voltages and the crankshaft and the connecting rods represent the driving voltages and their timing.*

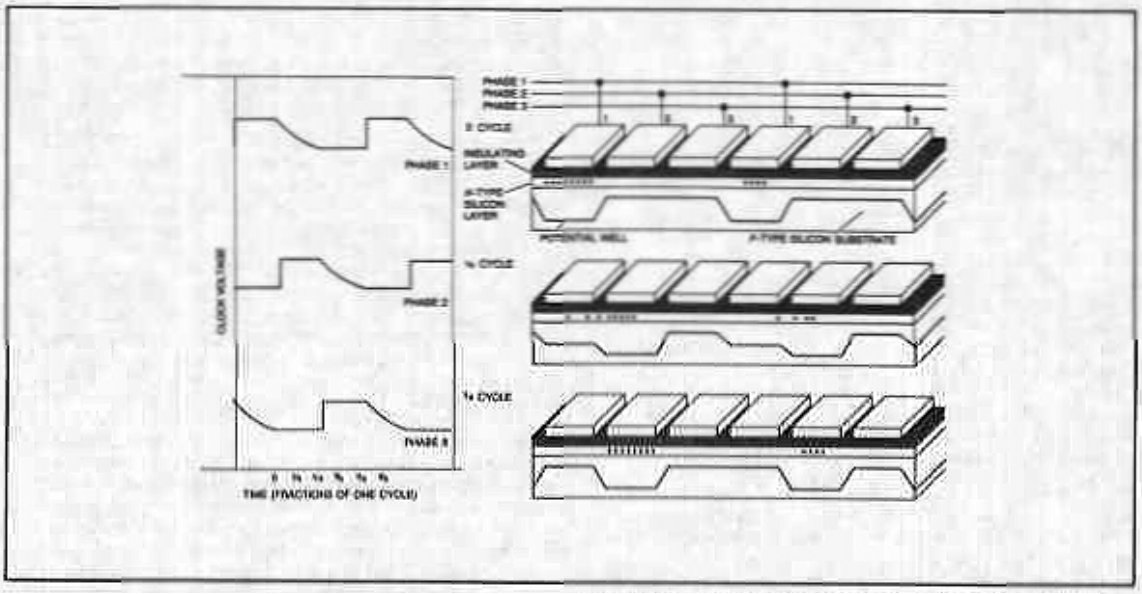
The electrons are induced to move to an adjacent region of lower energy (that is, a deeper potential well) by a combination of three influences: self-induced forces, field-aided forces and thermal forces. Self-induced movement results from the simple fact that a high-density packet of electrons (or any similar particles) tends to spread rapidly if the constraining force is removed, as is the case when the clock voltages change. This type of force is important during the early stages of charge transfer. Field-aided movement is important if the structure is designed in such a way that electric fields exist to assist the electrons' motion in the desired direction. This corresponds to adding a slope to the top of the pistons in the mechanical analogy. If such a force is present, it is important only toward the end of the charge-transfer cycle. Thermal forces arise from the fact that the electrons receive thermal energy from the silicon lattice and as a result are free to move about randomly. In their random motion they tend to move to regions of minimum electron energy. This type of force is important at the end of the transfer cycle only if field-aided forces are absent.

The self-induced force lasts for only a brief time at the beginning of the transfer cycle, but it is responsible for moving about 90 percent of a "saturation," or full, charge. If the field-aided force is present, it is responsible for moving most of the remaining charge at a rate directly proportional to the strength of the electric field and inversely proportional to the distance between the electrodes. If the field-aided force is not present, the remaining charge will move under the influence of thermal forces at a rate directly proportional to the temperature and inversely proportional to the square of the distance between the electrodes. This rate is usually lower than that resulting from the field-aided force, although at small dimensions it becomes increasingly significant because of its inverse quadratic dependence on distance.

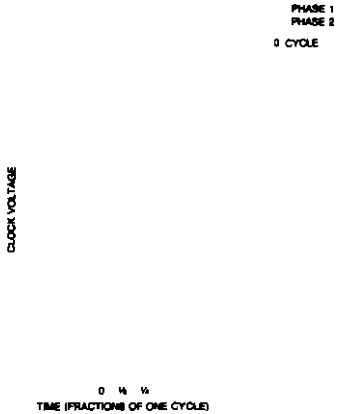
Although these forces are responsible for moving only a comparatively small fraction of the total charge packet, they are important because very little transfer inefficiency can be tolerated in practical devices. For example, if 1 percent of the charge is left behind at each transfer, most of a charge packet will have dispersed after only 100 transfers. In general the charge-transfer inefficiency must approach one part in 10,000 to be considered acceptable for most practical applications. In spite of this requirement, devices that can be operated at frequencies of up to 100 megahertz (100 million cycles per second) are possible if the structures ar made small enough. With modern microelectronic manufacturing techniques it is possible to design and build a charge-coupled unit cell with dimensions of less than a mil (a thousandth of an inch) on a side, although it is not always appropriate to do so.

Unit cells of such small dimensions are possible because of the simple nature of the charge-coupled structure, which does not require direct contact with the silicon in the array region. This arrangement is to be contrasted with conventional transistor technology, which in general requires several contacts per functional cell. Contacts consume a significant amount of valuable silicon because of the contact area and the tolerances needed to form a good electrical connection. From the manufacturing viewpoint it is this feature more than any other that makes charge-coupled devices so attractive.

The ability to generate, move about and detect many separate packets of electrons in a small piece of semiconductor material suggests that the charge-coupling principle can be applied to fulfill a number of information-processing requirements. In particular the highly ordered manipulation of charge packets characteristic of the operation of charge-coupled devices favors uses such as image sensing, computer-memory operation and sampled-signal processing. In each case the function is achieved by a proper combination of charge-coupled unit cells that operate individually exactly as described above.



conductivity of the silicon can be altered to form an "n



Three Two-Phase Charge-Coupled Elements *are shown in these cross sectional diagrams; again the curves give the relative timing of the clock voltages, this time for two-phase operation. Here the potential wells are given the required asymmetry by the introduction of different* n-*type conductivity regions just under the insulating layer. As in the illustration at the top, the external clock voltages on the electrodes cause the electrons to move in packets through the* n-*type semiconductor layer toward the right.*

Silicon, the semiconductor material of which charge-coupled devices are generally fabricated, is highly sensitive to visible and near-infrared radiation [*see illustration on page 9*]. In other words, when light falls on a silicon substrate, the radiation is absorbed (by means of the Einstein photoelectric effect), which results in the generation of electrons in a quantity proportional to the amount of incident light. If there is present an array of potential wells such as the one formed by charge-coupled devices, these electrons will fill the wells to a level corresponding to the amount of light in their vicinity. This "electro-optic" creation of electrons represents an input to the charge-coupled device that is entirely different from the input method required for the shift register discussed above and makes the charge-coupling concept useful for very different kinds of application Nonetheless, the packets of electrons generated by the light can be moved, just as in the shift register, to a point of detection and converted to an electrical signal representative of the optical image incident on the device. That signal, after some conditioning, can be displayed on a cathode ray tube. In this way a charge-coupled device can become the heart of a television camera

One of the significant advantages of charge-coupled image sensors over vacuum-tube sensors is the precise knowledge of the photosensor locations with respect to one another. In a camera tube the video image is "read" from a photosensitive material by a scanning electron beam. The position of the beam is never precisely known because of the uncertainty in the sweep circuits resulting from random electrical noise. In a charge-coupled sensor the location of the individual photosensor sites is known exactly, since it is determined during the manufacture of the component Such "metric" accuracy is important for proper alignment in color cameras and in applications requiring data reduction of the acquired image (as in photographic missions in space and photogrammetry).

It is generally convenient for purposes of discussion to separate charge-coupled sensors into two categories: linear sensors and area sensors. A linear image sensor is a simple straight-line array of photosensors with the associated readout and sensing circuitry. An area image sensor is a two-dimensional mosaic of photosensors, again with the associated readout and sensing circuitry

Linear image sensors are used for a host of applications, including air-to-ground and space-to-ground imaging, facsimile recording and slow-scan television The image to be viewed is obtained by providing relative motion between the sensor and the scene with the axis of the array perpendicular to the direction of the motion. A resolution of 500 or more photosensor elements is usually required. A primitive linear imaging device can consist of nothing more than a charge-coupled shift register and an output diode. In this structure the image is acquired when one holds the potential wells stationary by stopping the voltage clocks for some period of time (the "integration time") and then rapidly reads out the information by starting the clocks Such a simple charge-coupled device should be practical only in special applications that allow very long integration times The reason for this limitation is the "smearing" of the image that results when the shift register is clocked at the same time that it is illuminated.

A really practical charge-coupled linear image sensor is more complex. It consists of a photosensor array for accumulating the photocharge pattern plus an associated charge-coupled shift register with one charge-coupled element for each photosensor element in order to move the resulting charge packets to an output point. The elements of the photosensor array are individual charge-coupled storage elements with a common electrode called a photogate They are electrically separated from one another by a highly concentrated *p*-type region called a channel stop. The photosensor array is separated from the charge-coupled shift register by a region over which there is an electrode called the transfer gate.

In operation the photogate voltage is held high and the charge generated by the incident radiation (the photocharge) is collected by the individual photosensor elements. At the end of the integration time the transfer-gate voltage is raised from its normally low voltage condition. The charge-coupled shift-register electrodes adjacent to the photosensor elements are also brought to a high-voltage state. The photogate voltage is then lowered and the accumulated photocharge transfers to the shift register. After that is accomplished the transfer-gate voltage is lowered and the photogate voltage is brought back to its normally high state for another integration period. Meanwhile the charge-coupled shift register is clocked for the purpose of reading out the charge pattern.

A high-density image sensor is more economically designed with one shift register on each side of the photosensor array. Since there must be one charge-coupled element for each photosensor element, the distance between photosensor elements is equal to the distance between the shift-register electrodes for a two-phase charge-coupled shift register and is equal to 15 times the distance between shift-register electrodes for a three-phase charge-coupled shift register. In this example the signal charge from the two three-phrase shift registers is transported to a three-phase, two-element register

P TYPE SILICON

Potential-Energy Profiles *for a typical charge-coupled information-storage element are shown here as a function of distance into the bulk of the semiconductor at right angles to its surface. (In order to show the potential wells clearly, this diagram has been rotated by 90 degrees with respect to the preceding ones.) The charge-distribution patterns are shown for two situations: with no electrons in the well (top) and with some electrons in the well (bottom). As the curves indicate, the higher the clock voltage, the deeper the well.*

for delivery to the on-chip preamplifier. If two-phase technology is used, however, it is possible to shift the charge directly into an output diode, which is in turn the input to the on-chip preamplifier. Note that in either case the information-output rate of the device is twice the rate of either of the long shift registers. It is clear from this example that a two-phase charge-coupled structure not only is easier to clock but also is more economical to lay out for a practical device. Even though it is somewhat more difficult to manufacture because of the required asymmetry, it is likely to dominate future designs of charge-coupled devices when fully developed.

A linear sensor can be made to produce conventional two-dimensional images [*see illustration on next page*]. The image to be sensed is placed on a rotating drum, which provides the necessary motion of the image with respect to the device. The speed of rotation is synchronized with the vertical scan of the

The quality of image reproduction achievable with a linear charge-coupled sensor is excellent, reflecting the large dynamic range of the image sensor [*see illustration on page 31*]. The dynamic range is the ratio of the maximum to the minimum detectable image intensity. The quality of the reproduction demonstrates the very high transfer efficiencies and low electrical noise levels that can be achieved in existing charge-coupled devices.

Area image sensors are useful primarily for television-type camera applications. The image is obtained by conventional line-by-line scanning of the array mosaic and reproduction of the resulting video signal on a standard raster-scanned

photosensor elements in each column rather than by reading the odd and even elements in parallel, as in the case of the linear image sensor.

signal at the output. Finally, the entire operation begins again and is completed at regular intervals of a thirtieth of a second.

A typical image sensor designed to operate in this fashion consists of a rectangular 100-by-100 photosensor grid [*see illustration on page 22*]. Each photosensor element and associated readout electrode occupies only 1.9 square mils.

All 10,000 elements fit on a chip that measures .12 by .16 inch. An image taken with a camera system using such a device can be displayed on a television monitor.

This image-sensing device and others made by charge-coupled techniques are still somewhat primitive, but they clearly point the way toward a powerful camera technology. The combination of solid-state reliability, low-voltage operation, low power dissipation, large dynamic range, metric reproducibility and visible and near-infrared response offers to the potential user a compelling advantage over vacuum-tube image sensors and other solid-state image sensors.

The charge-coupling concept is basically one of semiconductor electronics rather than one of electro-optics. Because of the electro-optic characteristics of silicon, however, the light-sensing properties of charge-coupled arrays have tended to dominate this new technology. Nonetheless, the data-handling properties of such arrays may be of equal or even greater significance.

A charge-coupled semiconductor array is virtually ideal as a time-sampled analogue shift register. From the viewpoint of the electrical engineer this means a delay line where the delay is proportional to the readin/readout rate; if the array is long enough to contain the complete message, the readin and the readout rates can be different and the maximum delay available is limited only by the thermal generation of random electrons. At low temperatures several minutes of delay are possible.

As a memory or digital-storage device, charge-coupled arrays can perform the functions of sequential access or hybrid tasks such as drum or disk storage. The use of solid-state charge-coupled arrays to eliminate all mechanical motion and parts is a strong advantage of a memory consisting of charge-coupled devices.

The intrinsic analogue nature of the charge packet in a charge-coupled device suggests broad potential for application to sampled-signal processing. In a fundamental sense the use of charge-coupled devices as image sensors is merely a special application of the device as an analogue shift register.

If one restricts the definition of sampled-signal devices to those with an electrical (rather than an optical) input, then the predominant members of this class are variable delay lines and filters.

A delay line is a circuit that reproduces as accurately as possible an input signal delayed by a finite period of time. A delay line is "variable" if the time delay can be altered electrically The charge-coupled device acts as a natural delay line since any signal placed on its input diode will appear at its output in sampled form after the interval required for the charge packets to be shifted through all the elements of the structure. The charge-coupled device can be used as a delay

Relative Spectral Responses *of a charge-coupled silicon photosensor element (colored curve) and the human eye (black curve) are compared. The semiconductor material absorbs not only visible light (.4 to .7 micron) but also near-infrared radiation (.7 micron to 1.1 microns). The absorption of such radiation by a silicon substrate results in the generation of electrons in a quantity proportional to the amount of incident radiation. It is this "electro-optic" property that enables charge-coupled devices to be used as image sensors.*

Two-Dimensional Images *can be reproduced with the aid of a linear charge-coupled sensor in a variety of ways, one of which is outlined in this schematic diagram. The image to be sensed is placed on a rotating drum (left) whose speed of rotation is synchronized with the vertical scan of a conventional television display monitor (right). The charge-coupled device and the associated readout circuitry produce horizontal video lines at a rate rapid enough to build up a full-frame image on the screen of the monitor.*

Excellent Reproduction *obtained with a 500-element linear charge-coupled image sensor under widely varying light conditions is evident in these photographs. An apparatus similar to the one in the illustration on the opposite page was employed to scan the image. The photograph at left shows the original image to be scanned. The photograph at center shows the video display obtained from the charge-coupled system under optimum dispersion.*

way the charge-coupled device is said to perform a "buffer" function.

A charge-coupled delay line offers major advantages over the more conventional glass delay line and even significant advantages over the more exotic acoustic-surface-wave devices [see "Acoustic Surface Waves," by Gordon S. Kino and John Shaw: *Scientific American*, October, 1972]. Among these are wide dynamic range (better than 60 decibels after 30 television-display requirements

Extension of the simple delay-line concept leads to other sampled-signal processing devices. If a delay line is fabricated with interim taps at which the signal can be sensed and fed back to earlier stages in such a way as to affect the transmission of the data, then this structure can be used as a filter. Such a structure can be conveniently configured as a band-pass filter where the resonant frequency of the circuit is a direct function of the clock frequency. An improvement in the signal-to-noise ratio to within a decibel of the theoretical maximum has already been achieved.

Matched filters find application in wide-spectrum communications and in radar to detect weak signals in high noise backgrounds. In such applications charge-coupled devices will complement acoustic-surface-wave devices, which generally are useful only for delays of less than 100 microseconds.

As mentioned above, a charge-coupled storage element is capable of storing a packet of electrons with a varying amount of charge, depending on the design and operating conditions of the charge-coupled unit cell. Nonetheless, there is no reason one cannot conceptually quantize the charge-handling ability of the cell and view the device as a binary digital element. For example, one can arbitrarily say that if a storage element contains a charge less than half the saturation charge, it contains a "zero," whereas if it possesses a charge greater than half the saturation charge, it contains a "one." In this way the storage element becomes a memory "bit" and a charge-coupled delay line can be made to serve the function of a digital shift register or serially accessible memory. Since this function can be performed by other technologies also, one must ask what charge-coupling has to offer. The answer is cost-effectiveness. A charge-coupled memory not only has all the advantages of a conventional semiconductor component (compatibility with other electronic circuit elements, no mechanical motion, low power and voltage, variable clocking rates and other similar features) but also offers a potentially low cost-per-bit ratio approaching that of a magnetic memory. This is a result of the inherent structural simplicity of the charge-coupled device. By virtue of this simplicity, memory arrays as large as a quarter of a million bits per component on a piece of silicon less than half an inch on a side can be envisioned.

between a milliwatt and a watt to sustain it, excluding logic and other functions. The volume required for such a memory is less than that of a pack of cigarettes.

Another advantage lies in the fact that the charge-coupled device is basically analogue in nature. It is thus possible to store more than one data bit in each memory cell. This can be done by storing any one of a number of discrete levels of charge in each cell, thereby greatly increasing the information-packing density. For example, a 100,000-cell device capable of handling eight levels of charge is comparable to a 300,000-bit conventional memory. Such a memory chip would be of great value in digital-to-analogue and analogue-to-digital converters and other applications where multiple levels are achieved only by the addition of vast amounts of memory.

In view of these important prospective features of charge-coupled memory devices it appears that we are at the dawn of a revolution that will ultimately bring today's powerful digital computers directly into our everyday way of life. The charge-coupling concept, in short, is a major new innovation in semiconductor electronics. By virtue of its simplicity in design and fabrication, its high performance in terms of dynamic range and low power, and its high packing density and potentially low cost, the technology of charge-coupling will create major and unique new applications for the semiconductors that will have a direct impact on our lives.

CCD Fundamentals

No math—just a straightforward explanation of how CCD memory units and video devices operate and what they can do for you!

By Frank H. Bower

s called "charge-coupling." harge called "packets" are the silicon semiconductor called a "storage element," is e electrodes very close to the tion. By placing the storage n a line for instance, voltages an be alternately raised and al charge packets beneath torage element to the next cket may be of different size, a very simple analog shift shift registers, and because storage element to the next t, the amount of charge in the same, even after it has to as many as a thousand since the amount of charge in ing of charge packets can device is, in a sense, storing d as an electrical signal from e device at the end of the

the basic characteristic of essing and memory devices. ture by which information is register to allow operation in with currents and voltages ets manipulated in the CCD

nction utilizes another basic ductor devices. This is the e electrons are created in a photons in the approximate et) to 1100 (near infrared) onse peaks at about 800 h incident radiation in the portional number of free minated. If a silicon device rn of small but finite photo- r of free electrons generated directly proportional to the site. If the pattern of incident ight image from an optical rge-packets created in the faithful reproduction of the

e, during which the incident time and intensity propor- charge-packets are simul- coupling under an adjacent rallel CCD analog transport is called the transfer-gate

Figure 1: *Cockpit TV camera system.*

Each charge-packet corresponds to a picture element (pixel) and, when transferred to the adjacent CCD transport shift register, continues to faithfully represent the total sensed radiant energy which was absorbed in the specific photo site. The transfer gate is immediately returned to the non-transfer clock level (LOW) so photo-sites can begin integrating the next line of incident image information. At the same time, the CCD analog transport register, now loaded with a parallel-transferred line of picture information in the form of charge-packets from a line of sensor sites, is rapidly clocked to deliver the picture information, in serial format, to the device output circuitry.

The output circuitry consists of an output gate-diode structure and appropriate reset and buffering signal amplifiers. The output terminal delivers a sequence of electrical pulses, the amplitude of each being directly proportional to the charge-packet size generated in the photo-site where the charge-packet originated. Sample-and-hold circuitry, either on-chip or in the video processing support circuitry, delivers a line of video information.

Linear imaging devices (LIDs) sense and deliver information a line at a time; they are electronically scanned in one dimension and are often called line-scan devices.

Area imaging devices (AIDs) have an X-Y array of sense elements and sense an area image. They are built with both vertical and horizontal transfer gates and transport registers, and deliver an entire field of video information from each integration (exposure) period in the form of a series of lines of video signal.

CCD CHARACTERISTICS

• **Temperature.** The CCD works best at low temperatures. It has no problem at -55° C and can perform at full capability to +70° C. Above 70° C, storage-related parameters degrade rapidly due to physical properties of semiconductor materials. All semiconductor materials continuously generate hole-electron pairs due to thermal energy, even at room temperature. If there is a finite packet of electrons representing information in a storage element, and thermally generated electrons add to that packet over a period of time, the packet will become larger and eventually will no longer accurately represent the original information.

In image sensors, which are very high dynamic range analog devices, it is often desirable to provide cooling for low light level applications to reduce thermal electron generation. Since image sensor devices are used as single units or as a matrix of two to six devices, and dissipate on the order of 150 mW or less, cooling is relatively simple. In CCD memory, long registers could be a problem, so the devices are designed with "refresh" cells at frequent intervals in the register. These sense-and-restore cells detect the "1" or "0" at the output end of a shift register section before enough thermal electrons can be added to cause misinterpretation of the data. Practical economic considerations, however, limit the temperature range for CCD memory to about +70° C. Because of the very low power dissipated in CCD memory, it is practical to consider providing cooling to achieve economical military electronic systems.

• **Speed.** The speed limitation of CCD devices is theoretically that of electron mobility in silicon and experimental devices operating in the gigahertz range have been reported. Since surface-state trapping in the silicon slows the net mobility of carriers near the surface, "buried channel" devices are faster than "surface channel" devices. The practical limitation to operating speed is caused by the edge-dependent charging current associated with delivering the clock voltages to the capacitances of the shift-register gate electrodes (C dv/dt current). The clock-driver circuitry also dissipates increased power with increasing frequency of operation. Desired operating speed is, therefore, a very strong design consideration in determining how much of the clock driving function should be put on-chip, thus increasing chip temperature, or left for the system designer to provide on the board.

• **Reliability.** Since materials used and the fabrication and packaging technology for CCDs are essentially those of NMOS LSI products, CCD device reliability equals that of NMOS. CCDs are inherently lower power devices and, therefore, the occurrence of thermally-induced failure mechanisms should be lower than that of NMOS. Manufacture of CCDs utilizes state-of-the-art NMOS production technology for its N channel, silicon gate, ion-implanted, surface passivated structure. Packaging can be in any of the commercial or high-reliability packages already proven in industry.

• **Noise.** The basic CCD register, heart of all CCD devices, is practically noiseless because it does not have PN junctions as do MOS and bipolar devices. Associated on-chip charge detectors and buffer amplifiers do have PN junctions and introduce some noise. Dynamic ranges of 10,000:1 have been achieved without cooling.

Figure 2: *A two-phase CCD shift register. The two complementary clock voltage waveforms ϕ_1 and ϕ_2 are connected to alternate closely-spaced gate electrodes on the surface of the thin insulating layer on the silicon. A deep potential well which attracts electrons is created under the electrode clock voltage HIGH and disappears under the electrodes at clock voltage LOW. At t = 0, ϕ_2 voltage is HIGH and the finite charge packet of seven electrons is in the potential well under gate electrode #2 in storage element "A". At t = 1/2 cycle later, the potential well under gate #2 has collapsed due to ϕ_1 having gone LOW, and, since at the same time the adjacent electrode #3 connected to ϕ_2 has gone HIGH, the seven electron charge packet has been attracted to the new potential well under electrode #3. Another half cycle later, at t = 1 cycle, the potential well under electrode #3 has collapsed with ϕ_2 going LOW and the electron packet moves to the new well under electrode #4 which has gone HIGH with clock voltage ϕ_1.*

• **Radiation Hardness.** CCDs are not basically "hard." They are fabricated on very lightly doped, high-resistivity silicon which has characteristics more easily altered by radiation than the more heavily doped silicon in bipolar and conventional NMOS devices. Buried channel CCDs have been reported to be more radiation tolerant than surface channel devices. Government sponsored development programs are under way at several laboratories to investigate methods for radiation hardening CCD devices.

• **Packing Density.** CCDs have a three to five times packing density advantage over the next most dense MOS large-scale-integrated circuits. This is primarily because the basic CCD storage element requires no electrical contacts. The storage and transport of the information in the CCD register are performed by the pattern of conductive gate electrodes on the surface of the thin oxide layer over the silicon. The gates require much less area per storage element than the combination of gates and ohmic contacts required for an MOS storage element.

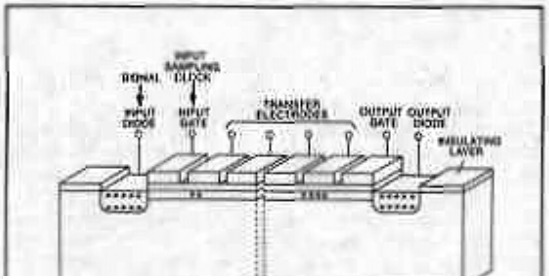


Figure 3: *Input and output diode/gate structures for electrical input and output to a CCD shift register.*

captured in the field of one of the sense elements. However, because of the time delay, they may arrive too late or in a sense element other than the one through which their exciting photon entered the silicon. The practical result is a loss of resolution or smearing of the image sensed. In some laboratories, work is being done to develop special CCDs for long wavelength IR image sensing.

All CCD image sensors consume low power and operate on low voltages. They are not damaged by intense light. Older devices will over-saturate and "bloom" under intense illumination but are not permanently damaged. Anti-blooming and exposure control is now available on more recent devices.

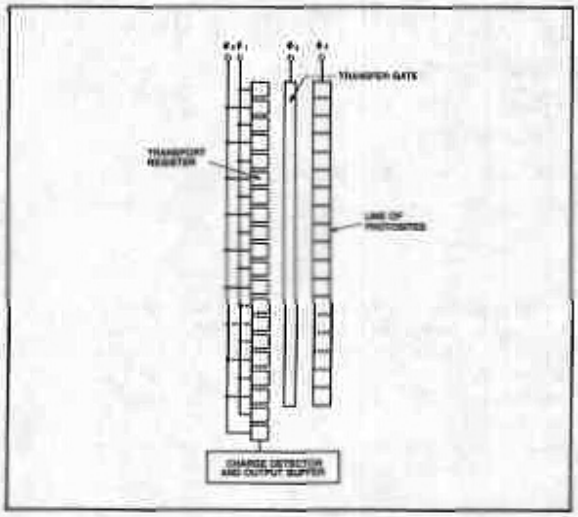


Figure 4: *Simplified block layout of a linear image sensor.*

Linear Imaging Devices (LIDs)

LIDs are configured as a single line of sensor elements on a long narrow chip. These devices are commercially available with 256 to 3,456 elements with longer devices in development. LIDs are used in facsimile machines or spectrometers where the subject is a line pattern. When relative motion of the scene with respect to the sensor is provided by other means, the array can present a high-resolution TV-type picture. A continuous real-time picture can be obtained from a LID sensor in an aircraft or satellite passing over the surface of the earth at a constant altitude and velocity. Using a scanning mirror in the optical system can accomplish a similar result. LIDs applications include:

- High speed, high resolution facsimile (text, maps, fingerprints, photographs)
- Aerial mapping with high measuring accuracy
- Real-time reconnaissance and surveillance
- Bar-code reading
- Sorting parts, mail, currency, food
- Conveyorized product non-contact inspection
- Automatic warehouse routing and palletizing control

Special configurations of LID in which the array is eight to 64 elements wide (rather than one element wide) can be used for Moving Image Integration (MII) applications and are particu-

larly effective in very low light level applications. Combined with analog delay lines, a LID can be used as the sensor for Moving Target Indication (MTI).

Area Imaging Devices (AIDs)
AIDs produce a TV picture. They are built in an array capable of being self-scanned in both the X and Y direction. These devices are available in 488 x 380 element arrays; they have also been built in other size array. As an example of a commercially available device, the Fairchild CCD222 is a 488 x 380 element array with a sense area format in a 3 x 4 aspect ratio for TV presentation. The device dissipates 60 mW when operated at a 7 MHz data rate, and operates at voltages of 12V to 15V. Its dynamic range is typically 1000:1 at room temperature. AIDs applications include:

- Low light level search and surveillance
- Missile and RPV guidance
- Star tracking
- Remote or projectile TV reconnaissance (Figure 5)
- Cockpit or gunsight camera
- Space telescope

Large area AIDs are difficult to produce "blemish free" at low cost. Industry is aggressively addressing reduction and elimination of random defects to achieve practical, low-cost volume-producible AIDs with chip diagonal dimensions in the order of > 0.50".

Figure 5: *Artillery launched TV system concept.*

Analog Signal Processors
The CCD has been shown to be a nearly ideal analog shift register. The simplest analog signal processor is a variable analog delay line where the delay obtained is a direct function of the clocking frequency and the number of storage elements in the register. Differential phase and differential gain of 1% or less is available in commercial devices. Tapped CCD delay lines are excellent sampled analog filters and can be externally programmed to change filter characteristics, scan a frequency spectrum, or provide correlation of weak signals in a strong noise background. CCD Analog Signal Processor applications include:

- Video and audio variable delay lines
- Moving target indicator filter
- Signal correlation and convolution
- Sonic imaging
- Voice compression and scrambling
- Video frame-grabber
- Communications and secure communications filter
- Scan rate converter
- Spread spectrum filter

Digital Memory
All CCD memories are basically serial because of the fundamental shift register nature of charge-coupling. They are dynamic memories which require periodic refreshing and, like other semiconductor memories, they are volatile. While their latency is greater than bipolar and MOS memory, they are as much as fifty times faster than magnetic disc and drum memories. Because of the shift-register nature of CCD, the CCD memory devices are block-access oriented rather than random bit accessed. The high bit-count per package allows use of distributed memory and changes in computer architecture. CCD memory applications include:

- Cache memory
- Signal analysis for sonar, radar
- Synthetic aperture radar memory
- Digital delay

Conclusion
Charge-coupled devices are now a family in production, bringing new capability to the military electronics systems designer. The high-volume, low cost production of area image sensors for TV sensing will require a combination of elimination of the causes of random defects from each step in the manufacturing process and improvement in the photo-lithographic techniques for patterning large area arrays so their area can be reduced without reducing responsivity

Volume production of high performance analog signal processing devices such as filters requires definition of a volume market sufficient to warrant the development costs and application of resources. Increased control of manufacturing processes, particularly accuracy of the photo-lithographic process or its electron-beam successor, will allow the dimensional control necessary to produce devices which are linear over a large dynamic range and have the high rejection characteristics desired.

Intensified CCD Camera Uses Fiber-Optic Coupling

by R.H. Dyck

Microchannel plates are imaging devices which are sensitive to charged particles and energetic photons. Originally developed for use as the amplifying element in military night vision systems, the microchannel plate is now finding its way into microscopes, oscilloscopes and solid-state cameras.

Figure 1: *Block diagram of the front end of the intensifier CCD camera.*

Figure 2: *Detailed drawing of the intensifier and the fiber-optic CCD.*

In view of the small fiber size compared to the size of the unit

device photograph (Figure 4). The vertical, lighter shade bars are aluminum strips on 30μm centers. Some of the preamplifier structure is visible through the fiber-optic faceplate in the upper right hand corner.

The quality of imagery produced by the CCD/fiber-optic faceplate combination is illustrated in Figure 5. For this picture, an image was formed on the front surface of the fiber-optic faceplate with an ordinary camera lens

Figure 3: *The CCD image sensor with its fiber-optic faceplate.*

Figure 4: *A photograph of a portion of the image sensor with its fiber-optic faceplate.*

Performance

The sensitivity of the camera is determined by the quantum efficiency of the photocathode, the intensifier gain, the CCD responsivity at the intensifier phosphor mean wavelength and the CCD noise or CCD background signal. Under some conditions, the sensitivity will be limited by the shot noise in the primary photoelectron stream For the smaller features in the image, sensitivity will also be limited by the MTF of the imaging system

The response spectrum of the photocathode is shown in Figure 6. This type of photocathode is called the S-20 extended red. Because of its high quantum efficiency in the red (600-700nm) and the near IR (700-800nm) compared to other available photocathodes, it is well suited to night vision applications. For example, where there is moonlight, this photocathode is desirable for its ability to sense a broad portion of the spectrum and thereby generate more total photocurrent.

For a second example, where there is some small amount of incandescent lighting, the red and IR responsivity of this photocathode takes advantage of the high output from lighting in that part of the spectrum The broadband responsivity is conveniently described in terms of photometric units using a standard 2854°K tungsten light source. The typical value is 200μA per lumen.

The gain of the image intensifier may be expressed in more than one way. The most common way is to give the photometric output per unit of photometric input. This takes into account the photocathode responsivity. Manufacturers give typical values of between 7000 to 15,000 footlamberts/footcandle. Here unity gain means that if one viewed the phosphor screen on-axis, the output would be one lumen per unit solid angle for every pi (3.14) lumens incident on the photocathode Since the angular distribution out of the fiber-optic backplate is more or less ideal ("Lambertian"), this is approximately equivalent to one lumen out per lumen in. Of course, this measure of gain requires that the type of light source be specified, in this case, it is again a 2854° K standard tungsten source

Another way to describe the gain would be to give the number of photons emitted from the intensifier (at the mean wavelength of the phosphor, namely, 560nm) per electron emitted from the photocathode. This measure of gain may be calculated to be 25,000 to 55,000.

Unfortunately, the intensifier camera has to suffer losses in quantum efficiency both in the photocathode and in the CCD, with the result that the predicted net increase in responsivity is of the order of 2000. As already noted, the reduction in the minimum illumination level onto the front end photosensitive surface, where the picture qualities appear most similar, has been found to actually be approximately 1000 times

The ability of the intensifier camera to faithfully reproduce details in scenery is limited in two different ways, just as it is in any video camera: by the Nyquist-limit resolution and by the MTF. The Nyquist limit resolution is a property of the CCD and is not altered by the intensifier. The MTF is the product of the MTF of the CCD by itself and that of the intensifier by itself As can be seen in Figure 7, the major MTF loss occurs in the intensifier. Nevertheless, there is useful MTF out to at least 25 line pairs/mm in the intensifier alone (≈5% MTF) and by the same measure, there is useful resolution in the CCD intensifier

Figure 5: *Image produced by the CCD with fiber-optic faceplate (without the intensifier).*

camera out to at least 23 line pairs/mm. Since the CCD raster measures 8.8mm vertically, this provides a useful resolution in the vertical direction of at least 400 TV lines. In the horizontal direction, *the MTF is greater than 15% at the Nyquist limit*

Overall camera performance is illustrated by some night scenes recorded with one of the cameras (Figures 8 and 9). An f/2.5 zoom lens was used wide open A nearly full moon was still rather low in the sky; the light meter read 0 35 lux at the car

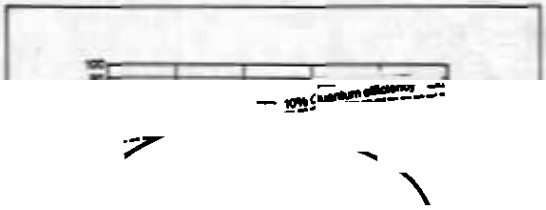


Figure 6: *Photocathode responsivity (Varo-S20/extended red).*

Figure 8: *Parking lot in moonlight.*

Figure 7: *MTF of the CCD222, the intensifier alone and the combination of the two.*

in Figure 8 and 0.15 lux where the man is standing in Figure 9. One-fifth of a second exposures integrate noise to approximately the same degree as is perceived by a typical observer.

There is a self-limiting behavior in the image intensifier: when the total intensifier output emitted (electron) current reaches the limit of the built-in power supply, the supply voltage drops so as to keep the average image intensity from the intensifier more or less constant. In the camera, at least for night scenery like that in Figure 8 and 9, the signal level in the CCD stays near the saturation level and only occasionally might a bright light in the scene cause the CCD to bloom. Because of this self-limiting feature, the camera behaves as if it had AGC and offers a good S/N ratio over several decades of average scene brightness.

Fiber-optic coupling

The use of fiber-optic coupling between the output phosphor layer of the intensifier and the CCD provides a coupling efficiency estimated to be in the neighborhood of 60%. Because the fiber optics are of the type designated numerical aperature (N.A.) 1.0in, the fraction of the omnidirectional light incident on the fibers themselves which exits from those fibers is close to 80%. Then each of the two fiber-optic plates (the intensifier backplate and the CCD faceplate) has a core fill factor that is about 85%. This gives a resultant efficiency of approximately 8 × 0.85 × 0.85 = 0.58 = 60%.

If, instead, a relay lens had been used, it would have been possible to improve the resolution somewhat by imaging the entire 18mm phosphor screen onto the CCD, but the coupling efficiency would have been considerably less.

In addition to this disadvantage of a lens coupler, there are the disadvantages of size and weight. This may add four inches or more to the camera length. For the case of a small primary lens, the weight of the front end portion of the camera might have been nearly doubled had a relay lens been used.

Acknowledgements

The author would like to thank Lee Ruzicka for major assistance in the designing of the prototype camera, in minimizing its noise, and in the characterization of the camera. The author would also like to thank Howard Murphy for many helpful discussions during the development of the camera.

FAIRCHILD WESTON

CCD IMAGING DIVISION

Technical Brief: Electrons vs. Voltages

Usually, when one talks about the output from a CCD image sensor or camera, they refer to so many volts or millivolts of output. It may be in regards to the saturation voltage, an output voltage, photoresponse non-uniformity, dark signal non-uniformity, responsivity or noise etc. All our data sheets talk in terms of voltages out. Some find it useful, however to talk in terms of charge, or electrons of signal rather than referring to voltages because it is electrons that are actually being moved about in the device. The voltage appears only as a result of converting this charge in the output amplifier.

The voltage at the output is linearly proportional to the number of electrons being converted. As a rule of thumb, our line scan CCD's output 1.0-1.5μV per electron of charge received, and the CCD222 about 2.5-2.7μV per electron. One may use this "scaling factor" to convert voltages back to electrons. For instance:

Parameter	Linear Imager Electrons	Area Imager Electrons
V_{OUT} = 50% V_{SAT} or Q_{SAT}		
NOISE (rms) (In Dark)		

FAIRCHILD WESTON

CCD IMAGING DIVISION

Technical Brief: Typical Internal Spectral Response (Smoothed)

Typical Internal Spectral Response (Smoothed)

R (mA/W)

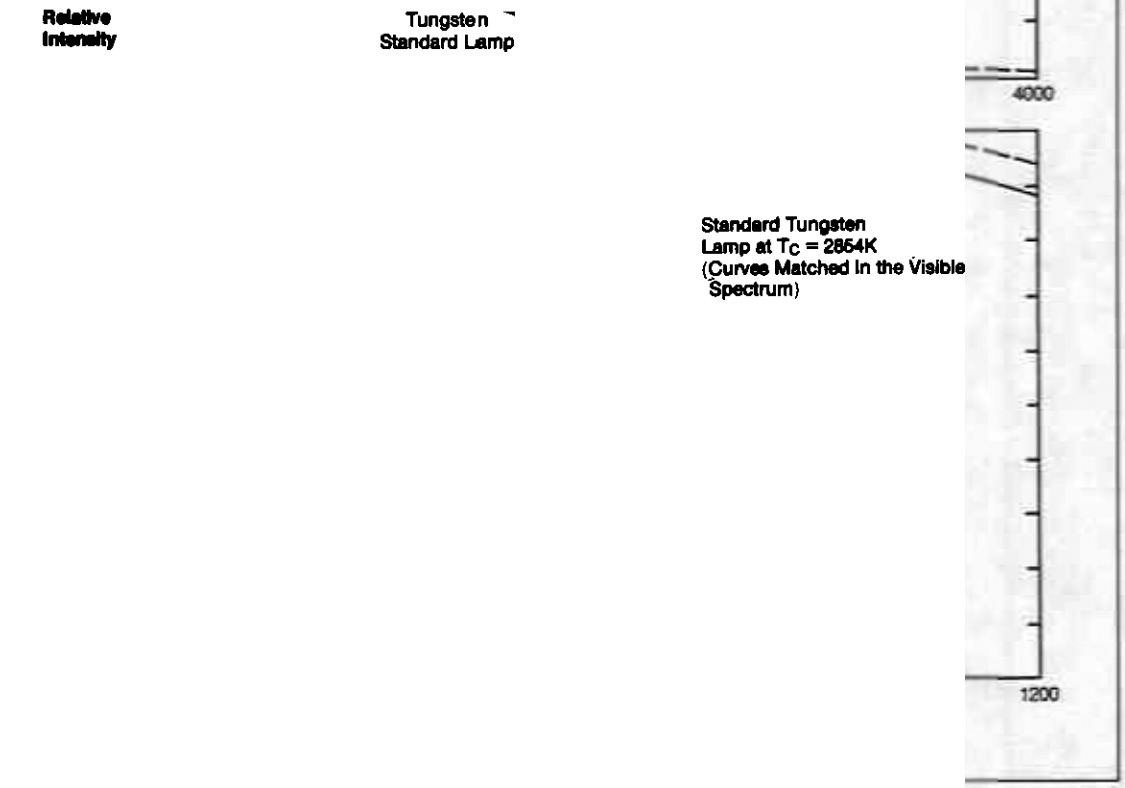
Line Scan Devices Type I: CCD111
Line Scan Devices Type II: CCD122, 123, 124, 133A, 143A, 153A, 151
Line Scan Devices Type III: CCD134, 145, 181
TV-Type Devices: CCD222

FAIRCHILD WESTON

CCD IMAGING DIVISION

Technical Brief: Spectra of Three Broadband Light Sources

Spectra of Three Broadband Light Sources



F700 Filter = 2.0 mm thick type BG-38 IR-absorbing filter (Schott Optical Glass Co., Dureya, PA).

F900 Filter = 3.0 mm thick type 1-75 IR-absorbing filter (Corning Glass Co., Corning, NY), or a 2.0 mm thick Schott KG-1 filter.

FAIRCHILD WESTON

CCD IMAGING DIVISION

Technical Brief: Charge Transfer Efficiency (CTE) Calculations

by D. Debe

Assume that the CCD photosites are uniformly illuminated. Also assume that every shift register element has the same charge transfer efficiency. Then:

$$\text{CTE (per 1 transfer)} = \left(1 - \frac{\eta\epsilon}{V_{OUT}} \right)^{1/i}$$

$\eta\epsilon$ is the global charge transfer inefficiency. V_{out} is the average pixel output amplitude under uniform illumination. (See sketch below); "i" is the total number of shift register elements (transfers) between pixel #n and the output amplifier. Note: each shift register bit consists of two elements; two transfers are required to move a charge packet through one shift register bit. Also, as shown below, there are more bits than the number of pixel lengths due to some extra bits (dark reference, prescan etc.) in the line of video.

The table below lists $\eta\epsilon$ versus CTE for each type of linear imaging device.

CTE (/1 Transfer)	CCD111 i = 259	CCD153A i = 523	CCD133A i = 1,035	CCD181 i = 2612	CCD143A i = 2,059	CCD151 i = 3,514	$\eta\epsilon$ UNITS
	$\eta\epsilon$	$\eta\epsilon$	$\eta\epsilon$	$\eta\epsilon$	$\eta\epsilon$	$\eta\epsilon$	
0.999 999	0.03	0.05	0.10	0.26	0.21	0.35	% of V_{OUT}
0.999 995	0.13	0.26	0 52	1 30	1 02	1 74	% of V_{OUT}
0 999 990	0.26	0 52	1.03	2 58	2 04	3 45	% of V_{OUT}
0.999 980	0.52	1 04	2 05	5.09	4.03	6 79	% of V_{OUT}
0 999 970	0.77	1.56	3.06	7.54	5 99	10 0	% of V_{OUT}
0.999 960	1.03	2.07	4.06	9 92	7.91	13.1	% of V_{OUT}
0 999 950	1.29	2 58	5 04	12.2	9 78	16.1	% of V_{OUT}
0.999 940	1.54	3.09	6 02	14.5	11.6	19 0	% of V_{OUT}
0 999 930	1 80	3.59	6 99	16 7	13.4	21 8	% of V_{OUT}
0.999 920	2 05	4 10	7.95	18.9	15.2	24 5	% of V_{OUT}
0 999 910	2.30	4.60	8 89	21 0	16.9	27.1	% of V_{OUT}
0.999 900	2 56	5 10	9 83	23.0	18.6	29 6	% of V_{OUT}

"Zero Reference Level"
DC Voltage Change
Due to Peripheral Response
and Photosite-To-Shift-Register
Optical Crosstalk

(n-5) (n-4) (n-3) (n-2) (n-1) (n) ◀— Last Pixel

FAIRCHILD WESTON

CCD IMAGING DIVISION

Application Note: Charge Injection

by D. Deba

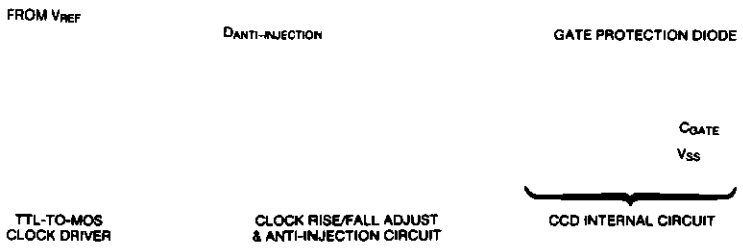
Every input pin has a gate protection structure which includes a diode from the input to the substrate (V_{SS}). Negative (transient) input voltages ($V_{IN} < V_{SS}$) will forward-bias the diode, injecting electrons into the bulk silicon of the CCD chip. (See Figure 1.)

If sufficient charge is injected, it will accumulate in the CCD analog shift registers and/or the photosites near the injecting gate protection structure(s). (See Figure 2.)

Injected charge which accumulates in the photosites will result in a bell-shaped increase in the apparent background dark signal, centered on the pixel nearest the injecting diode. Injected charge which accumulates in the shift register(s) increases the "register imbalance" ("odd/even"). The shift register nearest the injecting diode will have the larger output. (See Figure 3.)

The susceptibility to charge injection (sufficient to increase the background dark signal) and/or register imbalances varies significantly from device to device. It is not possible to select devices with "low" susceptibility. However, devices with low dark signal are typically more susceptible than devices with high dark signal.

FIG. 1 TYPICAL TTL TO CCD CLOCK INPUT INTERFACE CIRCUIT



NOTES:

1. $t_{RISE} \approx t_{FALL} \approx (R_1 \cdot C_{GATE})$
2. Do not use external parallel capacitor (C_1) to adjust t_{RISE}/t_{FALL}. Although this approach will work, C_1 acts as an A C shunt into the ground plane. This makes the ground plane very noisy.
3. See datasheets for actual C_{GATE} values for a specific CCD.
4. Plane Anti-injection diode and R_1 within one inch of CCD pin.
5. All diodes are FDH600 or equivalent.
6. V_{REF} can be generated by the following circuit.

FIG. 2 PHYSICAL EFFECTS OF CHARGE INJECTION:

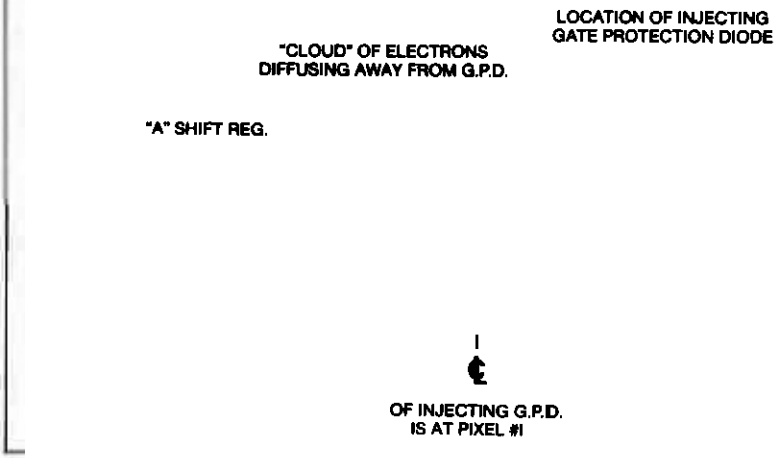


FIG. 3 V_{OUT} WITH CHARGE INJECTION AS SHOWN ABOVE (IN DARK):

FAIRCHILD WESTON

CCD IMAGING DIVISION

Application Note: Anti-Blooming and Integration Control

by T. Murphy and D. Debs

Problems solved by Antiblooming and Integration Control:
CCD image sensor performance in certain applications has been limited by one or more of the following:

1. CCD Responsivity could not be changed without changing the transfer clock cycle time ($t_{exposure}$), which generally is not acceptable in many imaging systems.
2. Photosite response could not effectively be "turned off" during part of each $t_{exposure}$. This degraded vertical resolution (MTF) and/or did not allow solutions of problem #1 above.
3. Very brightly illuminated photosites would "bloom"; or "smear" when oversaturated, causing a local loss of image resolution much larger than just the number of oversaturated photosites. (e.g. the CCD dynamic range was less than the image irradiance dynamic range.)

Features of Antiblooming and Integration Control:
The newest generation of Fairchild CCD image sensors (CCD134, 145, 181, etc.) contain two features to eliminate these problems. These features — "antiblooming" and "integration control" — can be used independently or in combination.

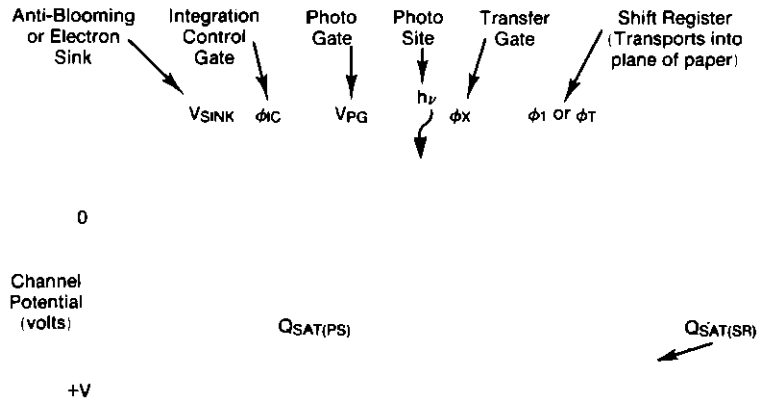
Antiblooming "clips" or limits the amount of charge that can be collected in any photosite. When properly adjusted, no photosite can accumulate more charge than the shift register can transfer properly. This causes a loss of signal amplitude information in the oversaturated photosites, but it prevents the oversaturated photosites from smearing into adjacent areas with consequent loss of resolution. Antiblooming alone has no effect on the performance (responsivity, etc.) of non-saturated photosites.

Integration control effectively reduces the responsivity of all photosites. This can be used to reduce all photosite charge packet amplitudes proportionately so that none of the photosites reaches saturation and/or blooms. Integration control functions as an electronically-variable "shutter" during each scan time.

Often the variable-responsivity feature of integration control is useful even if the blooming is not a problem. Integration control can be used for real-time adjustment of device responsivity to track line-to-line changes in object illumination, background reflectivity, vertical scanning speed, etc. Without integration control, this could only be accomplished by varying the transfer clock frequency ($f_{\phi X}$), which generally is not acceptable in fixed-output-rate systems. Adjustment of system responsivity by optical means (e.g. with a mechanical iris, mechanical shutter, and/or optical filters) is much slower than simply adjusting the integration-control clock cycle.

"Turning off" the photosite charge collection during each $t_{exposure}$ by clocking ϕ_{IC} also improves vertical resolution (MTF in the direction perpendicular to the CCD array long axis.) This is particularly advantageous when the object is moved in a start/stop "stepped" mode.

Figure 1A: ϕ_{IC} = 0 volts; No Anti-blooming or Integration Control



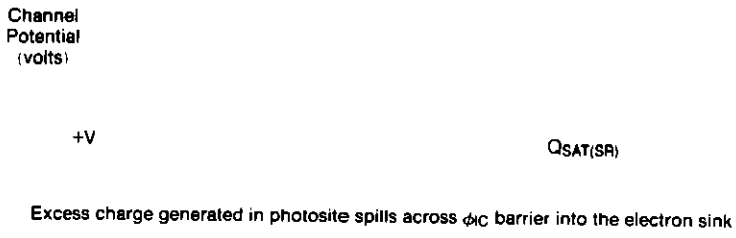
Light shield omitted for clarity in Figures 1A, 1B, & 1C.

Implementation of these Features:
The ϕ_{IC} pin controls both the antiblooming and integration control features. Figure 1 shows the behavior of charge generated in the photosites for three different ϕ_{IC} voltages. Charge is represented by the shaded areas and by the small circles or dots.

In Figure 1A, the ϕ_{IC} is biased at zero volts. In this case, the charge storage capacity of the photosites ["$Q_{SAT}(PS)$"] is larger than the amount of charge that the shift register can transfer without excessive loss ["$Q_{SAT}(SR)$"]. If the charge in photosite #n ["Q(n)"] is excessive [e.g. if $Q(n) > Q_{SAT}(SR)$], then the excess charge will remain in this shift register cell when the shift registers are clocked. This excess charge will combine with the charge packet from the #(n+2) photosite, thus "smearing" the information down the shift register. If the excess charge combined with the information from the #(n+2) charge packet exceeds $Q_{SAT}(SR)$, then the remainder will combine with the photosite #(n+4) charge packet, etc. If [$Q(n) > Q_{SAT}(PS)$], then the excess charge will also bloom within the photosite array into the #(n+1) and #(n–1) photosites, etc.

Blooming can be eliminated by biasing the ϕ_{IC} at approximately the same voltage as the photogate (V_{PG}). (The exact voltage required for optimal antiblooming operation is a function of device manufacturing tolerances. See below for recommended adjustment procedure.) Figure 1B shows this condition. Charge generated in the photosites in excess of $Q_{SAT}(SR)$ spills across the barrier formed by ϕ_{IC} into the electron sink.

Figure 1B: ϕ_{IC} Bias ≈ V_{PG}; Antiblooming Enabled



Excess charge generated in photosite spills across ϕ_{IC} barrier into the electron sink

Figure 1C: ϕ_{IC} Bias ≥ (V_{PG} + 3V); Integration Control Enabled

All charge generated in photosite spills into the electron sink when ϕ_{IC} Bias ≥ (V_{PG} + 3V).

If no charge collection (integration) is desired during the first part of the scan (integration) time, then ϕ_{IC} is clocked to a clock-high voltage at least about 3V higher than the photogate voltage. This is shown in Figure 1C. All charge generated during this time will spill into the electron sink. The control of the duty cycle of photosite signal charge collection is called "Integration Control." See Figure 2 for a typical timing diagram.

Reduction of the effective integration time by integration control effectively shifts the dynamic range of the device to a higher integration range. Figure 3 shows the typical dynamic range for $t_{int}/t_{exposure}$ ratios of 0.1 to 1.0. Minimum $t_{int}/t_{exposure}$ ratio is limited by optical crosstalk from the photosites into the shift registers during the ϕ_{IC} clock-high time (e.g., when the photosite-generated charge is being dumped into the electron sink.)

Antiblooming can be combined with integration control by setting ϕ_{IC} clock-low to approximately the V_{PG} bias voltage per the procedure below.

Optimization of Antiblooming

To optimize antiblooming, first set ϕ_{IC} to zero volts. Increase integration by increasing irradiance or $t_{exposure}$ until the device output is almost V_{SAT}. Then increase ϕ_{IC} DC bias voltage or ϕ_{IC} clock-low voltage to the highest voltage which does not diminish the output signal amplitude. (See figure 4).

Figure 2: Integration Control and Anti-Blooming

(Note 2) | (Note 3)

(Note 4)

NOTES:

1. $t_I > (t_{fall}$ of $\phi_X)$
2. All charge generated in photosites during t_{IC} is dumped in V_{SINK}.
3. All charge generated in photosites < Q_{SAT} during t_{INT} is transferred into the shift registers during ϕ_X clock-high period. Photosite charge > Q_{SAT} (shift reg.) generated during t_{INT} goes into V_{SINK} if anti-blooming voltage is optimized
4. ϕ_{IC} clock-low = 5 to 7 volts will give best anti-blooming operation
5. ϕ_{IC} t_{rise} & $t_{fall} > 4\mu s$ to minimize clock coupling of ϕ_{EC} into V_{OUT}
6. To eliminate integration control, but retain anti-blooming ϕ_{IC} = +5 VDC
7. To eliminate both integration control and anti-blooming, ϕ_{IC} = 0VDC or V_{SS}(−2V)
8. To use integration control without anti-blooming, use ϕ_{IC} clock-low = 0.0 to 0.7 volts and ϕ_{IC} clock-high = same range as ϕ_T or ϕ_1 clock-high voltage.

Figure 3: Dynamic Range vs. $t_{int}/t_{exposure}$ Ratio

Irradiance During $t_{exposure}$ (J^*/cm^2)

1 25 .5 .75 1

$t_{int}/t_{exposure}$ Ratio

*For the CCD145 device illuminated by a standard 2854° K tungsten lamp with

Figure 4: Maximum Output Voltage vs. ϕ_{IC} Voltage

FAIRCHILD WESTON

CCD IMAGING DIVISION

Application Note: Photosite Transfer Loss (PSTL)

Introduction

Two phenomenon affect the transfer of charge packets from the photosites to the output amplifier. Photosite Transfer Loss (PSTL) degrades the transfer of charge packets from the photosites into the CCD shift register(s). Charge Transfer Efficiency (CTE) describes the transfer of charge packets along the CCD shift register(s) into the output amplifier gated charge integrators.

CTE

CTE is specified on every CCD data sheet. It is approximately a constant percentage of the V_{signal} over at least the 1%-to-100%-of-V_{sat} range. CTE is not normally affected by the amplitudes of charge packets transferred through the CCD shift register(s) during previous scans.

PSTL Significance

PSTL is often assumed to be negligible. This assumption is reasonably valid for applications where (1) the minimum pixel illumination is at least 5-10% of V_{sat}, and/or (2) where the pixel amplitudes are to be digitized to ≤ 10 gray scales (≈3 bits analog accuracy of full scale) Such applications generally include document scanning for facismile or PC inputs, OCR, and some industrial inspections.

PSTL can significantly reduce degrade device performance under the following conditions:

1. Device in dark or very dim illumination for many successive integration times.
2. Accurate signal information is required for pixel inputs in the (0.01% to 5-10%) of E_{sat} range. (e.g. a high system dynamic range is needed.)

These requirements are typical of satellite and telecine applications. Our newer devices have much better PSTL than standard devices.

Before discussing PSTL amplitudes further, a definition of PSTL is given

PSTL Definition

The effects of PSTL are shown and defined in Figures 1 and 2 below. The CCD is not illuminated for a long time (t_{dark}). Then the light source is switched on, coincident with the beginning of a CCD integration time (t_{int}). Radiant flux amplitude (light intensity) is held constant for at least three successive t_{int} periods before the light source is turned off. (LED lamps are a convenient source for this test.) Note that the CCD output waveform (V_{out}) is delayed by one t_{int} period (one "scan") from the illumination clocking. If the CCD had PSTL = 0, then the average pixel output amplitude (V_{signal}) resulting from each illuminated t_{int} would be the same. If 0 < PSTL ≤ (100% of V_{signal}), *then the V_{signal} resulting from the first illuminated t_{int}* will be attenuated.

The charge lost from the first illuminated scan by PSTL is gradually transferred out of the photosites after the illumination stops. A measure of this slow, exponentially-decreasing charge leakage is defined as the "vertical charge transfer inefficiency" or "VCTIE" in Figure 1.

PSTL Causes and Cures

PSTL is caused by three mechanisms:

1. Slow electron charge traps in the photosite regions. (Absorb charge quickly, release charge over many scans.)
2. Inadequate time and/or electrical field gradients to transfer charge from photosites to shift registers.
3. Subthreshold depletion of photosites over many scans while device is in dark.

The effects of slow traps and subthreshold depletion can be significantly reduced (better than 2x improvement) by adding optical bias light or "fat zero" to the incident illumination. Use of optical bias is limited by the noise contributions. See Table 1 below. An optcal bias of ≈20mV decreases PSTL by at least 2x while increasing noise by only ≈25%.

Inadequate time and/or electrical field gradient can be improved by (a) provide a longer ϕ_X pulse, per Figure 3A below, and/or (b) by also clocking the photogate (V_{PG}) per Figure 3B below.

Recently designed devices (CCD134, 145, 181) have negligable PSTL: < 5% of V_{signal} for |(1% of V_{sat}) ≤ V_{signal} ≤ (100% of V_{sat})|. Older devices may have up to an order of magnitude larger PSTL.

Optical Bias		Total Noise in Dark*
(mV_{RMS})	(ke^-_{RMS})	(ke^-_{RMS})
		.32

*t_{int} = 1ms, f_{data} = 2MHz, no C.D.S., Output Scale Factor = 1.25μV/e^-, average dark signal ≈4 mV/ms, T_P=+25°C. (Typical for 143A, etc.) Note that (Peak-Peak Noise) ≈ 5x (RMS Noise).

Figure 1: Effects of PSTL and Vertical CTIE

Figure 2: Effects of PSTL and V-CTIE in a typical Line-Image-Sensor-Based X-Y Scanning System (in "pushbroom" mode)

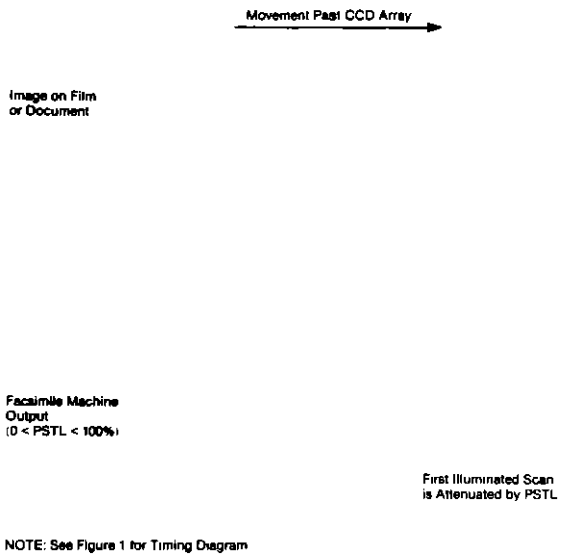


FIGURE 3: OPTIMAL CLOCK TIMING TO MINIMIZE PSTL

CCD145, 181:

ϕ_{PG} ("V_{PG}")

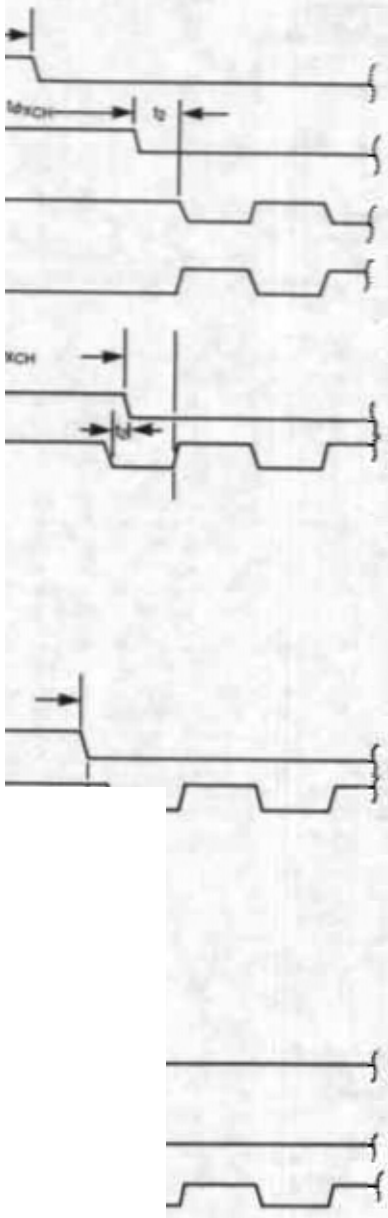
CCD122, 133A, 143A, 153A:

ϕ_X

ϕ_T

CCD123:

(Note 2)



4. $t_3 \geq 50$ ns

5. $t_4 \approx 1\ \mu s$.
6. $t_5 \geq 1\ \mu s$.
7. $t_{\phi PGCH} \geq 2\ \mu s$.

FAIRCHILD WESTON

CCD IMAGING DIVISION

Application Note: CCD Input and Output Requirements

CLOCK INPUTS

Clock Load Characteristics
CCD clock inputs range from relatively large capacitive loads (30-1000pF, depending on device size) to very small capacitive loads (<5pF). DC leakage current into all clocked inputs is negligible ($\leq 1\mu A$ at +15V).

Recommended Clock Drivers
Standard TTL-to-MOS clock drivers, such as the National *Semiconductor DS0026*, are recommended for driving the high-capacitance inputs They are also convenient for driving the low-capacitance inputs with appropriate resistance between the 0026 and the CCD.

Clock Rise/Fall Times
Refer to Figure 1: "Typical TTL-to-CCD Clock Input Interference Circuit". The damping resistor R_1 limits the t_{fall} time so that the CCD pin does not "ring" below V_{SS}. (Momentary pulses more negative than V_{SS} may degrade CCD performance by increasing the apparent dark signal. See the "Charge Injection" application note for further details)

Excessively fast clock rise and fall times will also degrade CCD performance by increasing the internal clock coupling into the output waveform and/or increasing the external clock coupling into the P.C. board ground plane(s). Rise and fall times should exceed 30ns whenever possible.

P.C. Board Layout
The TTL-to-MOS clock drivers and interface circuitry should be located close to the CCD (within 1 inch if possible) to reduce transmission line "ringing" problems.

Although the DC currents into the CCD clock inputs are negligible, large surge currents are required at the clock transitions. Decouple each clock driver IC with a large local capacitor between V_{CC} and ground.

On devices with separate substrate (V_{SS}) and signal (V_{SG} or V_{GG}) grounds, provide separate ground planes on the PC board

Combining Clock Inputs
Many devices have two shift registers which can be run in parallel. It is preferable to run both shift registers with the same clock drivers unless the combined capacitance is too large for the clock drivers. Running both shift registers with the same clock drivers will improve CCD performance by reducing the number of clocks which can capacitively couple into the CCD substrate.

Damping Circuits to Avoid
The gate-to-gate capacitance of the CCD transport and transfer gates (ϕ_1, ϕ_2, ϕ_T, VT, ϕ_X, ϕ_{PG}, etc.) is usually a significant part of the total gate capacitance. Internal clock coupling can degrade device performance if the effective impedance of the clock-driver-plus-damping circuit is excessive. A particularly bad damping circuit for these gates is back-to-back diodes See Figure 2 for details.

These diodes are intended to slow down the CCD gate rise and fall rates as the gate approaches the final clock-high and clock-low voltages. However, they also act as a very high impedance between the clock driver and the CCD gate during the first ~0.7V of internal gate-to-gate clock coupling. This can permit internal gate-to-gate clock coupling to become so large that it degrades CTE and/or the output waveform. (See Figure 1 for a recommended damping circuit)

2-Phase Shift Register Clock Requirements
Devices with two-phase shift register clocks (ϕ_1 and ϕ_2) have special requirements on their phase relationship.
(See Figure 3.)

DC INPUT VOLTAGE SUPPLY REQUIREMENTS

CCD Noise Immunity
The CCD has minimal built-in noise rejection. Noise on the V_{DD}, V_{RD}, and V_{SG} supplies is attenuated by $\leq 50\%$ at the CCD *signal output(s)* (V_{OUT} or *OS*). Also, ϕ_1, ϕ_2, or ϕ_T clock coupling into V_{OG} will increase register imbalance.

All DC input voltages should be well regulated and thoroughly decoupled to ground. If the device has separate substrate (V_{SS}) and signal (V_{SG}) grounds, then all output amplifier supplies (V_{DD}, V_{RD}, V_{OG}, V_{BIAS}, etc.) should be decoupled to V_{SG}.

Typical DC Bias Currents

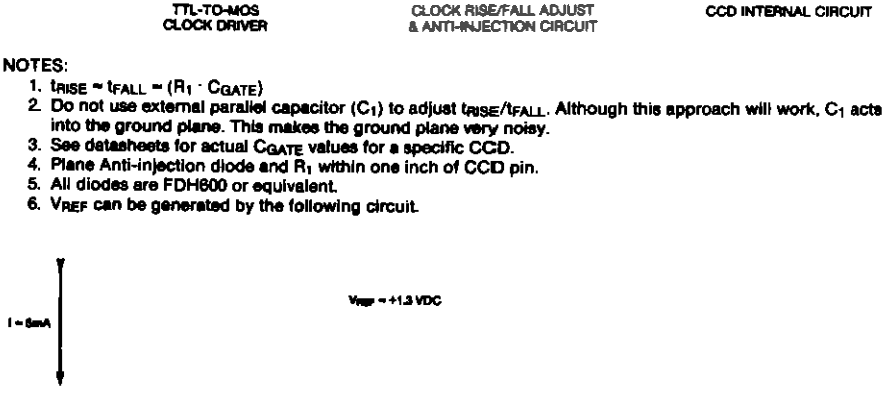
Pin Name	Typical Current*	Comments
V_{DD}	3-10mA	$V_{DD} = V_{CD}$
V_{CD}	3-10mA	
V_{RD}	$<1\mu A$	Normally derived by resistor dividers from V_{DD}
V_{OG}	$<<1\mu A$	
V_{PG}	$<1\mu A$	
V_T	$<1\mu A$	Large decoupling capacitance required due to large V_T-to-ϕ_T internal capacitance.

*See data sheets for specific values

BUFFERING OF CCD OUTPUTS

The on-chip amplifiers are designed to drive a low-capacitance, high impedance external buffer. Maximum output load is ≤ 10 to 20pF and $\geq 5k\Omega$ to V_{SS} or V_{SG}. An emitter follower or equivalent is recommended.

FIG. 1 TYPICAL TTL TO CCD CLOCK INPUT INTERFACE CIRCUIT



NOTES:

1. $t_{RISE} \approx t_{FALL} \approx (R_1 \cdot C_{GATE})$
2. Do not use external parallel capacitor (C_1) to adjust t_{RISE}/t_{FALL}. Although this approach will work, C_1 acts as an A.C. shunt into the ground plane. This makes the ground plane very noisy.
3. See datasheets for actual C_{GATE} values for a specific CCD.
4. Plane Anti-injection diode and R_1 within one inch of CCD pin.
5. All diodes are FDH600 or equivalent.
6. V_{REF} can be generated by the following circuit.

FIGURE 2: DAMPING CIRCUIT TO AVOID

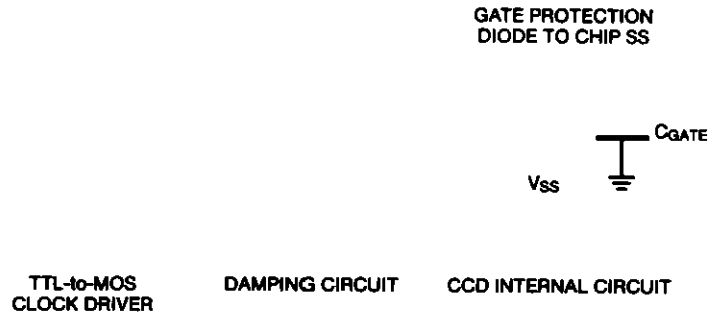
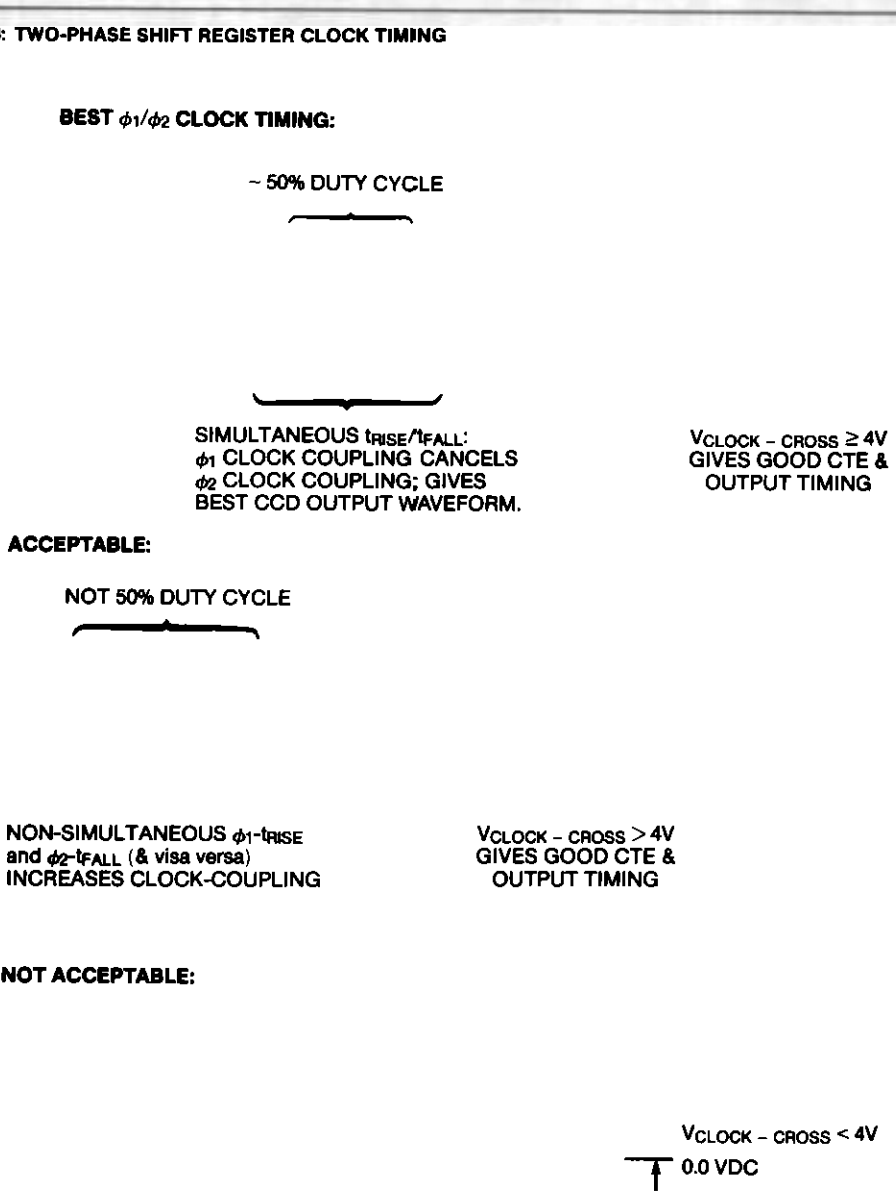


FIGURE 3: TWO-PHASE SHIFT REGISTER CLOCK TIMING



FAIRCHILD WESTON

CCD IMAGING DIVISION

Application Note: Correlated Double Sampling

by T. Murphy

A technique called Correlated Double Sampling (CDS) is recommended when very low noise performance is desired. CDS is the differencing of samples of the zero reference level (V_{REF}) and valid video taken at each pixel. In order to use CDS the internal sample-and-hold circuit must be disabled and an external reset clock must be used. An explanation of the CCD output circuit and the advantages of CDS follows.

The CCD output circuit converts the photoelectron signal charge to a voltage signal. Charge packets from the photosites are transported to a precharged diode whose potential changes linearly in response to the quantity of signal charge delivered. This potential is applied to the gate of an n-channel MOS transistor producing a signal at $VIDEO_{OUT}$. A reset transistor driven by the reset clock (ϕ_R) recharges the charge detector diode to the positive potential V_{RD} before the arrival of each new signal charge packet.

Figure 1 shows the three output waveform components: reset clock capacitive feedthrough, zero reference level (V_{REF}) and valid video. The potential difference between V_{REF} and valid video is proportional to the signal charge.

When the diode is reset to V_{RD} there is a thermal noise voltage component in addition to the nominal potential. The square root of the variance of this reset noise voltage is V_{RMS}.

$$V_{RMS} = \sqrt{\frac{kT}{C}}$$

where k is Boltzmann's constant, T is temperature in °K and C is the capacitance of the node. At room temperature this represents about 200μV of noise

The reset noise can be eliminated by CDS. The same random reset noise voltage is present in both V_{REF} and valid video. By taking the difference between samples of V_{REF} and valid video for each pixel the random voltage is eliminated. See Figure 2 for a block diagram of the CDS circuit.* See Figure 1 for the timing diagram.*

The filter in Figure 2 serves to reduce high frequency noise before sampling. If the filter is not employed, the differential amp increases the high frequency noise in the sampled signals negating the benefits of CDS The filter is a low-pass filter with a cut-off frequency of approximately 3 times the video data rate. This allows for a relatively sharp transition from V_{REF} to valid video while still reducing the high frequency noise

Another advantage of CDS is that it reduces the 1/f noise in the output at frequencies below f_{DATA}. Since each pixel has independent V_{REF}, there is a very short time scale for readout of the signal. Therefore the low frequency noise in the device's internal output amplifier and in V_{RD} is effectively filtered out.

For ideal supression of 1/f noise the V_{REF} and valid video sampling internals (Figure 1) should be very close together. In practice, and especially at high data rates, the valid video sample may be taken later in the pixel to assure that the signal has settled. Maximum signal-to-noise ratio is realized by integrating V_{REF} and valid video samples for as long as possible without sampling reset feedthrough or the V_{REF}-valid video transition.

*It is not recommended to use one sample and hold while attempting to clamp V_{REF} as is displayed in Figure 3. Clamping to ground makes the CDS circuit very susceptible to noise and ground loops in the "ground plane."

FIGURE 1. TIMING DIAGRAM

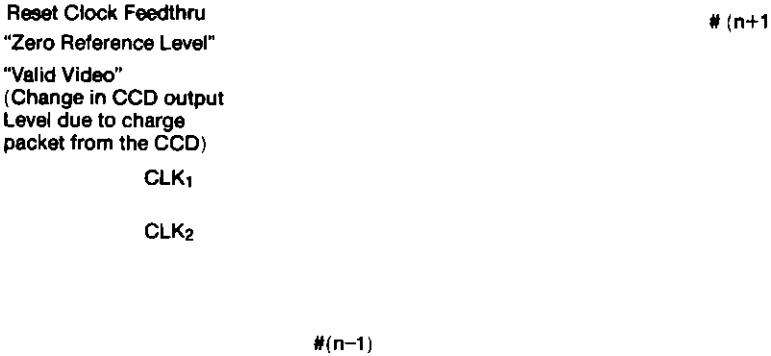


FIGURE 2. BLOCK DIAGRAM

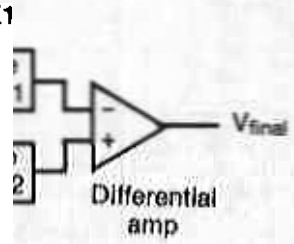


FIGURE 3. COR

INCORRECT SETUP

FAIRCHILD WESTON

CCD IMAGING DIVISION

Technical Brief: Position of Pixel #1 vs. Package Edge

POSITION OF PIXEL #1 vs. PACKAGE EDGE & PIN #1

18-Pin Sidebrazed	0.295±.020	±.060	0.145±.010	±.025	0.0±1.0	±10.0
	0.089±	±.045		±.045	0.0±	± 3.0
				±.045	0.0±	± 3.5
24-Pin Sidebrazed	0.210±.010	±.025		±.025	0.0±	± 3.0
	0.299±	±.037	0.295±	±.036	0.0±	± 2.6
	0.292±		0.295±		0.0±	
28-Pin Sidebrazed	0.158±	±.067	0.295±	±.047	0.0±	
	0.154±				0.0±	
				±.041	0.0±	± 3.6
24-Pin Sidebrazed	0.424±	±.037	0.295±	±.036	0.0±	± 2.6
	0.170±				0.0±	

Note: Special selections for

FAIRCHILD WESTON

CCD IMAGING DIVISION

Application Note: Comparison of The "C" and "R" Line Scan Camera Families

History

Availability of the first member of the commercial ("C") line scan camera family, the CCD1300C, was announced in 1977 by the CCD Imaging Division, which was then a part of Fairchild Semiconductor Corporation. The family was broadened between 1977 and 1980 by announcement of other members of the family; the CCD1100C, the CCD1200C, the CCD1400C, and the CCD1500C. In addition to design and development of the new family member to provide customers a choice of camera resolutions ranging from 256 to 2048 elements, significant engineering efforts were successfully aimed towards reducing the manufacturing costs and consequently the customer prices for the line scan camera products, to provide improved camera performance, and to adapt the standard line scan cameras for a variety of application-specific situations for a number of valued customers.

The improved "C" cameras were well received by the market place, but they were not ideal for industrial uses. The camera enclosures were not sealed nor of optical instrument quality, the cameras could operate only at data rates below 10 MHz per second, and the control unit-to-camera cable length had to be less than 2 meters for good performance. Certain integrated circuits used in the family were archaic, and were consequently obsoleted and made unavailable by our vendors in and before 1985.

A first "industrial" grade, or "R" family line scan camera was developed and announced in 1979 while CCD Imaging belonged to the Fairchild Semiconductor Division of Schlumberger. This camera was specifically designed for factory installations, was sealed for environmental protection, and was packaged in an enclosure only 2.25 inches in diameter and 5 inches in length.

The "R" camera family has been broadened by announcement of several new products between 1979 and 1986 and the family of products have been continuously improved in offered performance capabilities. The family now includes the 512 × 1 element CAM1200R, the 1024 × 1 element CAM1300R, the 2048 × 1 element CAM1500R, and the 3456 × 1 element CAM1600R. A controller, the CB1000R, for drive and interfacing of any of the cameras and systems including a camera and the CB1000R and a cable set are available as CCD1200R, CCD1300R, CCD1500R, or CCD1600R. These products are still supplied by the original CCD Imaging Division, which has become an important part of Fairchild Weston Systems, Inc., which is a Schlumberger company and is organizationally separated from Fairchild Semiconductor.

R-To-C Family Comparisons

The obsolete "C" commercial-grade line scan cameras were sold in diamond shaped vented sheet metal enclosures about 6 inches in length, 3 inches in width, and 5½ inches high. The enclosures were optically imprecise, and the sensor alignment, with respect to the mounting mechanisms provided on the enclosure, was somewhat unpredictable. The camera enclosure was not sealed, and the electronics and internal optical components could be damaged by exposure to high humidity conditions and by dirt and dust.

The "R" industrial-grade line scan cameras were available in sealed cylindrical enclosures 2¼ inches in diameter and 5 inches in length. The sensor package is precisely and rigidly attached, with a circular printed circuit board, to the camera faceplate.

The "C" cameras contained logic circuits for full control of sensor timing plus an analog video processor for interface to the user system. The "R" cameras are very flexible operationally; all timing is controlled by two clock signal inputs which permit the cameras to be operated optimally for any specific application. The two time-division multiplexed video outputs of the "R" cameras (one for the CAM1600R) permit user-design of video circuitry meeting the needs of the camera system, while the video processor included in the "C" cameras met only data sheet specified interface conditions. The "C" cameras could be driven with cables not longer than 6 feet in length at their maximum data rates of 10 MHz; the "R" cameras include line drivers and receivers which permit operation at cable lengths of > 250 feet at 20 MHz with twisted pair clock cables.

The "C" cameras were recommended for use only with a control unit and power supply unit made by Fairchild. The "R" cameras can be easily controlled by customer-provided clock and power supply inputs, and they are strongly recommended for OEM installations

Fairchild Weston, however, provides at a low price, the CB1000R controller which is adaptable for use with any member of the "R" camera family. As is well documented in the preceeding CB1000R data sheet, the controller provides a very flexible set of clock signals to the attached camera, provides the dc supply inputs needed by the camera, and includes an analog "video processor" and a "pixel locator." The video processor provides, at its BNC-connector outputs, a de-multiplexed element-sequential ground referenced 0-1 V peak analog video output signal at a 75 ohm impedance level.

The "pixel locator" run-length encodes the camera data, and eases the task of interfacing a camera to a computer for image processing.

It is recommended that a complete camera system (512 element CCD1200R, 1024 element CCD1300R, 2048 element CCD1500R, or 3456 element CCD1600R) be ordered because of the inherent convenience and economy in receiving a fully integrated system. The "CCD----R" systems provide all of the functional performance features which were available from the "C" cameras when the pixel locator accessory was also purchased, and offer many performance improvements as well. OEM camera users are encouraged to specify Fairchild Weston Model CAM1200R, CAM1300R, CAM1500R, or CAM1600R to obtain only an industrial-grade camera with a resolution of 512, 1024, 2048, or 3456 elements respectively. Owners of one of the "R" cameras are encouraged to order a CB1000R for use with their cameras—it may ease design-in of the camera into an electro-optical system.

The "C" family of Fairchild Weston line scan cameras has, as do all high technology products, become obsolete. The "C" family is replaced by the superior "R" family of line scan cameras made available by the pioneering efforts of the CCD Imaging Division of Fairchild Weston Systems, Inc.

FAIRCHILD WESTON

CCD IMAGING DIVISION

Application Note: The Synchronous Flash Mode For The 3000 And 5000 Series Cameras

by J. Solari

INTRODUCTION

Sometimes it is valuable to get a picture of a moving object (perhaps an object on a moving belt). To accomplish this, the object is illuminated by a short intense flash in an otherwise dark environment. Under these conditions, a small amount of light may leak under the light shield covering the vertical shift register and create a 'ghost' image in the shift register. The vertical shift register runs continuously and will move that image some distance up the register before photogate transfer occurs.

This 'ghost' image can be eliminated by inhibiting the vertical shift register clocks to the sensor during and after the flash, until the photogate clock transfers charge from the pixels to the registers. In this way, the real image is superimposed on the ghost image, and the ghost is not seen.

OPERATION

To eliminate the ghost image, supply a TTL level start pulse to reset the central timing gate array, before the flash occurs. A low to high transition (recommended rise time <100ns) resets the gate array, which triggers a new field index as seen in the attached timing diagram. The vertical clocks to the sensor are inhibited from reset time until the next normal photogate transfer time, which occures 18 lines after reset. After the start pulse is sent into the camera, the actual reset may not occur immediately; wait one horizontal line time, then fire the strobe light within the first 17 line times.

SPECIAL TIMING CONSIDERATIONS

Operation of the camera in the flash mode does not affect RS170 output, however, resetting the camera does. Therefore, any frame grabber accepting the output of the camera should also be triggered from the start pulse. When the camera is operating in a standard RS170 mode of operation, the maximum rate for strobe flashing is 30/sec, interlaced; 60/sec, non-interlaced or pseudo-interlaced. The camera may also be operated in the flash mode with external clock inputs, with a maximum flash rate of one flash per frame. The camera may not be operated in the flash mode while in gen-lock.

I/O CONNECTIONS FOR CAMERAS FACTORY PRE-SET IN THE FLASH MODE

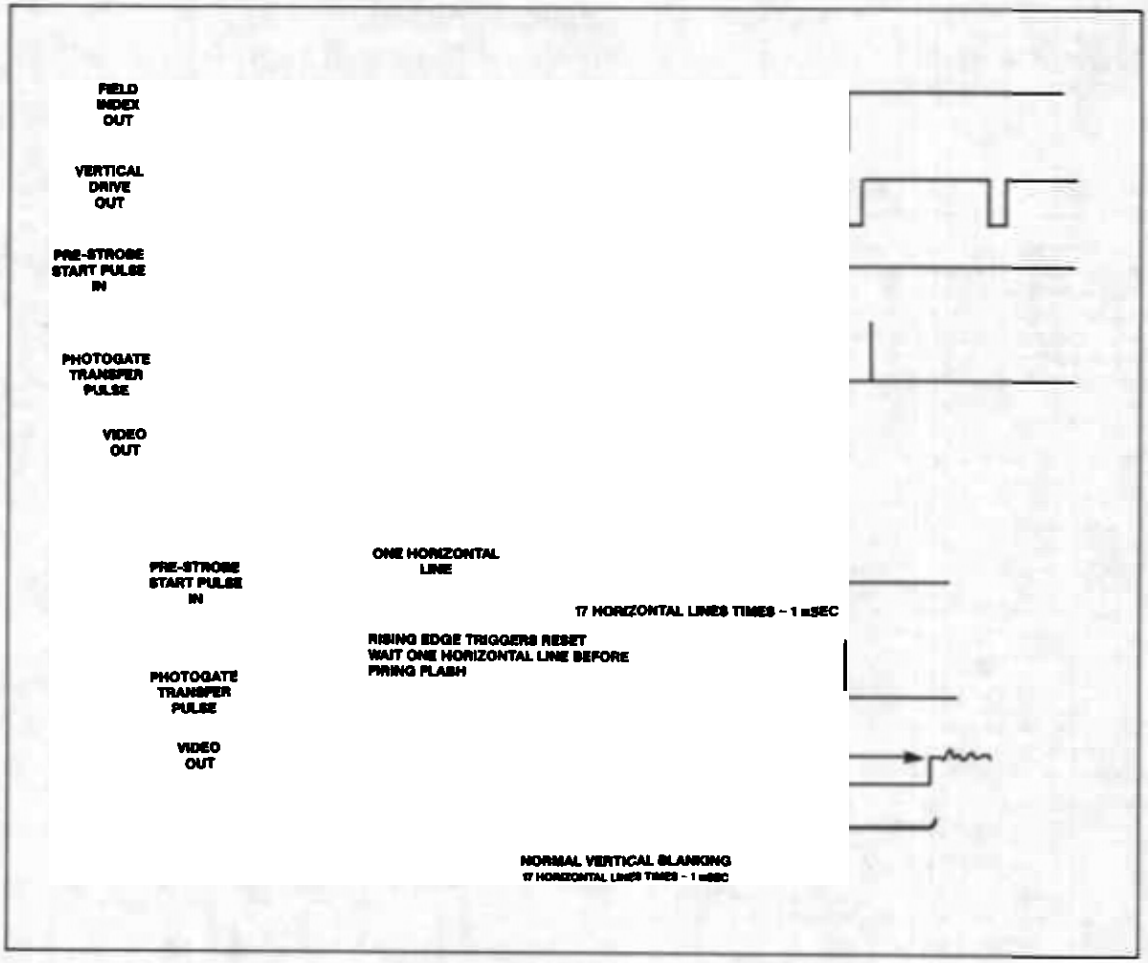
3000 Series Cameras which have been pre-set at the factory for the flash mode allow access for the input of the start pulse through pin #13 of the 25 pin 'D' connector.

5000 Series Cameras which have been pre-set at the factory for the flash mode allow access for the input of the start pulse through pin #2 of the user I/O connector.

MODIFYING STANDARD CAMERAS FOR THE FLASH MODE

The 3000 Series Cameras built since 1985 marked with a serial number beginning with 'C', include a Fairchild gate array logic board and are capable of being used in the synchronous flash mode. This mode may be invoked by grounding pin #24 of the gate array. A start pulse must be supplied to the reset pin (#20) of the gate array. This pulse may be accessed into the camera through the 25 pin 'D' connector, by isolating pin #13 of the connector (previously ground), and connecting it to the reset pin of the gate array. Pin #13 must be freed from ground both in the power supply and on the rear mother board of the camera.

The 5000 Series Cameras may be used in the flash mode by installing a jumper at W4 G-H, and supplying the reset pulse to pin #2 of the 25 pin user I/O connector. (Detailed instructions are in the CCD5000 Manual, Sections 3.1.5 and 3.1.3)


FIELD INDEX OUT
VERTICAL DRIVE OUT
PRE-STROBE START PULSE IN
PHOTOGATE TRANSFER PULSE
VIDEO OUT
PRE-STROBE START PULSE IN
ONE HORIZONTAL LINE
17 HORIZONTAL LINES TIMES ~ 1 mSEC
RISING EDGE TRIGGERS RESET
WAIT ONE HORIZONTAL LINE BEFORE
FIRING FLASH
PHOTOGATE TRANSFER PULSE
VIDEO OUT
NORMAL VERTICAL BLANKING
17 HORIZONTAL LINES TIMES ~ 1 mSEC

FAIRCHILD WESTON

CCD IMAGING DIVISION

Application Note: Predicted Effects of High-Power and High-Energy Optical Irradiance on CCD Image Sensors

This technical note describes the predicted effects of large concentrations of radiant optical energy on Fairchild CCD image sensors—such as might occur with a laser or a solar image. It should be understood that these are only predictions; we do not know of actual instances of such damage. All of the effects are thermal; that is, this technical note only deals with heating effects due to dc or pulsed radiation that is concentrated in some definable way. The emphasis will be on worst-case conditions.

As a point of reference let us first consider how much heating will typically occur when a device is uniformly irradiated near saturation at some common integration period. We will only treat the case of monochromatic light at a central wavelength, namely, 600nm, and we will only consider one typical device, namely, the CCD133. The area of the dark ceramic header (90% absorbant) is approximately 4.5cm². At the data sheet test condition of 1ms integration period, with the device near saturation the radiant power absorbed by the device can be estimated to be, based on data sheet information:

$$0.9\ (0.4\mu J/cm^2)\quad (4.5cm^2)/10^{-3}s = 1.6mW$$

(The saturation energy density of 0.4μJ/cm² was calculated by dividing the typical saturation voltage of 2.0V by the typical spectral responsivity at 600nm of 5V/μJ/cm².)

A rough estimate of thermal resistance of the package is 10° C/W. Therefore the estimated rise in temperature is:

$$1.6mW\ (10°\,C/W) = 0.016°\,C$$

If the radiation is confined to the area of the silicon chip (0.2cm²), which has an average absorbtance of only about 20%, the corresponding values are:

$$0.2\ (0.4\mu J/cm^2)\ (0.2cm^2)/10^{-3}s + 8\mu W$$

and

$$8\mu W\ (10°\,C/W) = 0.00016°\,C$$

Let these two temperatures be our point of reference. Next let us consider several representative specific examples of high energy optical irradiance.

Case 1. The sun is focused on the device. In one specific scenario an F/2 lens forms an image of the sun 2.3mm in diameter on the CCD133 chip. The luminous intensity of the solar image is:

$$\frac{\pi\ (1.6 \times 10^9\ lumen/steradian.\ m^2)}{4F^2}$$

$$\frac{=3.14\ (1.6 \times 10^9)}{4\ (2)^2} = 3.2 \times 10^9\ lux$$

Using our recommended 700 nm infrared blocking filter, one lux equals approximately 0.33mW/cm², giving a power density of 100W/cm² and a total incident power of 3.2W. Taking the absorbtance to be 20% (as we did above for the mostly aluminized chip) the total absorbed power is approximately 0.64W and the temperature rise of the chip above the ambient is approximately

$$0.64W\ (10°\,C/W) = 6°$$

Since the device is rated at 125° C maximum, there is no danger at all of harming the device, assuming there is adequate control of the ambient temperature.

Case II. A laser spot 10μm in diameter is focused on the chip. The question is: What are the power and pulsed energy limits before something gets too hot? For this case, it is useful to think of the silicon chip as a large heat sink on which is an insulating glass layer 1-3μm thick, and an aluminum layer 1μm thick. The aluminum can absorb power faster than it can spread laterally and downward to the single crystal silicon heat sink. If the aluminum layer reaches a temperature of 450° C for even very brief times like a few minutes, it is possible to damage the device. (This occurs at the aluminum - silicon contacts.) For laser pulses less than 20-50ns, the power would not spread significantly outside the 10μ spot and one can calculate the incident energy required to heat that amount of aluminum by 450 - 25 = 425° C. In addition to the information we already have, we need the heat capacity of aluminum, which is 2.4J/cm³° C. The critical energy level is then

$$\frac{2.4J/cm^3°\,C\ (10^{-4}cm)\ (425°\,C)\ (8\times10^{-7}cm^2)}{0.1} = 0.8\mu J$$

For pulses longer than 20-50ns, this critical energy will increase because the heat has time to spread, but simple quantitive predictions are probably not reliable because of the complexity of the chip structure.

General Observation. Since the silicon chip can withstand 125° C indefinitely and 450° C for very brief periods of time, and since CCD devices typically saturate at illumination levels that heat the device by less than 0.1° C, it is clear that there is at least a 1000:1 safety margin above saturation before damage will occur

FAIRCHILD WESTON

CCD IMAGING DIVISION

Application Note: X-Ray Imaging with Fairchild CCD Image Sensors

by R.H. Dyck

X-ray imaging is conventionally done with either photographic film, X-ray phosphor screens viewed directly, or X-ray image converter tubes coupled to a vidicon-type of television camera. Solid state image sensors can provide several advantages over the conventional approaches. For example, by simply replacing the tube-type camera by a solid state camera one achieves the advantages of:

1) a distortion-free scanning raster,

2) an ultra-stable scanning raster, and

3) full digital control of the image readout, as is desirable for interfacing to digital systems.

The above example can be implemented in two ways. One way is to use relay optics to image the output of the X-ray image converter tube onto the image sensor. Because sensitivity is generally quite important, the aperture of the lens should be approximately f/1.4 or larger, i.e., a smaller f/no. The other way is to use an image sensor with a fiber optics faceplate and a converter with a fiberoptic backplate. An improvement in sensitivity of 10 to 20 times has been achieved with this approach. In terms of numerical aperture (NA), the aperture of this type of coupling can be approximately 1.0; this is approximately equivalent to f/0.5.

Other approaches to X-ray imaging with solid state image sensors are: (1) to use an X-ray phosphor that is deposited directly on a fiber optics faceplate on the sensor, and (2) to let the X-rays excite the sensor directly. This last method is not recommended, however, since the X-rays incident on an image sensor, especially when it is powered, lead to degradation of the device similar to the way devices degrade due to any other form of high energy radiation such as gamma rays and high energy electrons. The effects include (1) increased dark signal, (2) decreased charge transfer efficiency, and (3) drift in optimum drive voltages. Depending on the particular type of radiation, the dose, the device and the temperature, any one of these effects may dominate.

Where X-ray imaging directly on the sensor is considered, the following information may be of value.

1) The attenuation depth in silicon varies strongly with X-ray energy. Above approximately 6 KeV, the characteristic attenuation depth (where the incident X-ray flux is attenuated 2.72 times) is greater than 30 μm. This situation results in relatively larger crosstalk between photoelements, and also in the possibility of poor uniformity of response.

2) Continued exposure to X-rays, especially while under power, causes the device to degrade. Near room temperature, this will generally be detectable at 10^3 to 10^4 rads, and may make the device unusable at 10^5 to 10^6 rads. Annealling will *restore proper performance to some degree, but since the* best annealling only occurs at temperatures above the maximum recommended storage temperature, low-risk annealling treatments are not expected to help very much. Annealling assisted by ultraviolet irradiation may be considerably more effective.

3) Because good imaging is only expected for relatively low X-ray energies, and because the normal glass window on the image sensor strongly attenuates these low-energy X-rays, it is important to replace the glass window by a thin beryllium cover (of course, for ultraviolet-assisted annealling a beryllium cover would need to be removable)

4) Dosimetry. A rad is defined differently in silicon device investigations relative to the conventional definition for biological and health studies. For the latter, the definition is 100 ergs/gram in carbon. For silicon devices, it is 4.2×10^{13} electron-hole pairs/cm^3 in silicon. Another useful relationship in dealing with radiation effects in silicon devices is that it takes approximately 3.5 eV of energy, on the average for high energy radiation, to create one electron-hole pair in silicon.

5) Active area. Because the aluminum that shields the CCD registers from light is transmitting for X-rays, the registers may be stopped during an exposure, and the active area may be considered to include the registers. This situation results in oddly shaped element areas for line-scan imagers unless elements are paired. For paired elements, the resulting active element area is approximately $26 \times 260\ \mu m \approx 0.007$ mm^2.

6) Example of an X-ray exposure and the resulting radiation dose. Assume 10 KeV radiation. Each X-ray photon will generate approximately 3,000 photoelectrons. Of these, 2,000 will be generated in the first 100 μm of depth. Assume all 2,000 will be collected. Assume an average exposure of 50 X-ray photons per $26 \times 260\mu$m pixel. This will generate approximately 100,000 photoelectrons or approximately 10% of the saturation output voltage. This exposure, expressed in radiometric units, is

$$\frac{(50\ \text{photons})\ (10^4\ \text{eV/photon})\ (1.6\times10^{-19}\ \text{joule/eV})}{7\times10^{-5}\ \text{cm}^2} = 1.1\times10^{-9}\ \text{j/cm}^2.$$

The radiation dose seen by the upper portion of the device can be estimated as follows: assume a characteristic absorption length of 100 μm. The absorption coefficient is then one percent per micrometer. The excitation density at the top of the device and for the average exposure used in this example is then

$$\frac{(50\ \text{photons})\ (3000\ \text{pairs/photon})\ (0.1/\mu\text{m})\ (10^4\ \mu\text{m/cm}}{(7\times10^{-5}\ \text{cm}^2)\ (4.2\times10^{13}\ \text{pairs/rad})} = 5.1\ \text{mRad}$$

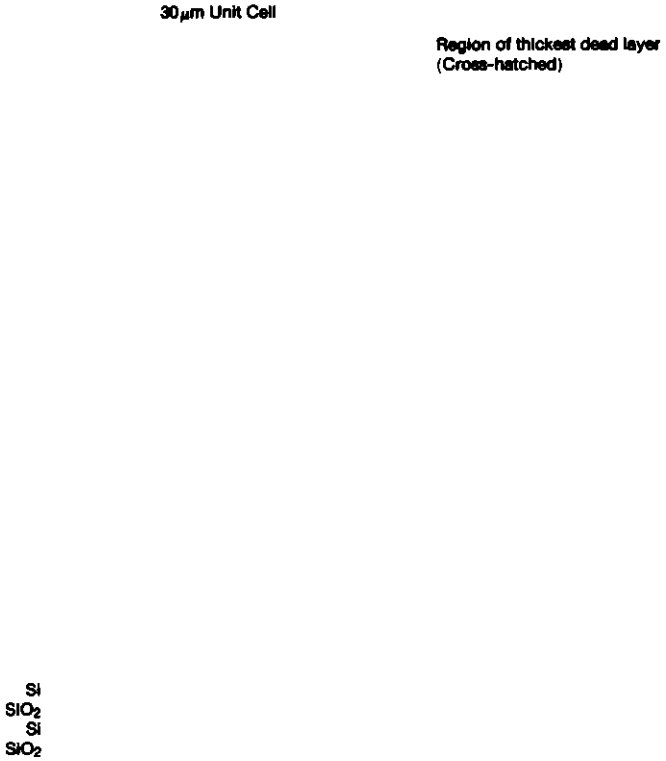
Therefore, if one is careful not to expose the device unnecessarily to the X-ray source, it should be possible to take as many as 200,000 exposures before the significant degradation resulting from 10^3 Rads accumulated dose will occur.

FAIRCHILD WESTON

CCD IMAGING DIVISION

Technical Brief: Dead-Layer Structure of the Standard CCD222

DEAD-LAYER STRUCTURE OF THE STANDARD CCD 222 RELATIVE TO HIGH-ENERGY PARTICLE-SENSING APPLICATIONS



FAIRCHILD WESTON

CCD IMAGING DIVISION

Technical Brief: Questions and Answers

Q: What are the length of die tolerances and pixel size tolerances on our linear imaging devices? What is the center-to-center pixel spacing error?

A: The "pitch" of a CCD linear image sensor is defined as the center-to-center photosite spacing. The pixels and thus the pitch are defined initially on the die by the first masking operation.

cumulative pitch error is $\pm 0.00006\mu m$/pixel*, which is equivalent to $\pm 0.065\mu m$ total for 1,024 pixels at $13\mu m$ pitch. (i.e., the CCD133) (All data above is worst-case.)

The second source of pitch inaccuracy is expansion or contraction of the silicon die between first mask in wafer

*Cumulative pitch error is equal to the total length block error divided by the number of pixels in the block.

Q: What light sources are recommended for use with CCD's?

A: Any light source in the visible spectrum is recommended for use with CCD's. Usual choices are "daylight fluorescent", or filtered tungsten. Tungsten has some IR content which should be filtered out for best results.

contrast is acceptable, some near IR light sources may be used.

Q: How long an integration time is necessary to acquire an image using a CCD?

CCD Imaging
Quality Assurance Program

Introduction
CCD Imaging's quality assurance program has been developed to ensure the products with the highest standards of quality and reliability are manufactured and delivered to customers. These quality standards are designed not only to meet those required by CCD Imaging, but also to meet or exceed contractual obligations. The program covers all activities including new product development, manufacturing process controls, control of vendors and subcontractors, and the review and inclusion of special customer requirements Every functional group manager is responsible for implementing and monitoring conformance to CCD Imaging's quality assurance program.

To produce quality products, a documented plan and a system of controls and monitors is necessary. CCD Imaging has used appendix A of MIL-M-38510 as a model for their quality assurance program. Some of the major aspects of this program are described in the following sections.

Document Control
CCD Imaging document control department has three basic functions:

- **Control of Procedures, Drawings and Specifications**
  Documents related to materials, manufacturing processes, testing and product qualification are maintained by document control. Each is uniquely numbered and identified by function, category and revision status.
- **Change Control**
  Any change to a procedure, drawing or specification must be documented and approved by the appropriate functional groups (including customers when applicable) before implementation. A history of all changes is maintained by document control and the revision status is identified on each document.
- **Records Management**
  Records of product manufacturing, inspections, screening tests, qualifications, quality conformance inspections and audits are retained for a minimum period of three years or as specified by customers.

Training
Although every position is staffed with qualified, experienced personnel, training is an integral part of CCD Imaging's operations and includes the following techniques or methods:

- On the job training for assigned operations.
- Classroom presentations and individual or group discussions.
- Oral and/or written tests.
- Participation in selected courses of study or seminars.
- Records of training are maintained and these are updated after periodic re-training or other kinds of training are completed.

Maintenance and Calibration
Measuring or test equipment used in the manufacture or testing of products at CCD Imaging are periodically maintained and calibrated in compliance with requirements of MIL-STD-45662. Records of calibration are maintained and the standards used are traceable to the National Bureau of Standards. The calibration status of each piece of equipment is indicated by a sticker that identifies the date of calibration, calibration due date, and the name of the organization that performed the calibration. Equipment not requiring calibration or that are used for reference are indicated by a sticker.

Process Controls
Manufacturing and quality ensure that all processing operations are accomplished using documented product flows, lot travelers, specifications, approved materials, environmental controls and qualified production equipment.

- **Incoming Inspection**
  Received materials are sample inspected for acceptance per applicable specification and criteria. Records are maintained by vendor and type of material and may include the results of actual "use" tests or verification of material composition of construction.
- **Final Inspection**
  All products are 100% visually inspected and tested to documented criteria that are specified for each type of product. Quality inspects and accepts based on sampling plans derived from MIL-M-38510 (LTPD's), MIL-STD-105D (AQL's), or to appropriate MIL-STD-883 methods.
- **In-Process Inspections and Audits**
  Manufacturing inspects and monitors the results of each manufacturing process using documented acceptance criteria, comparison to standards or process monitoring materials. Results are recorded on travelers, data logs or trend charts for the purpose of: identification and removal of non-conforming materials as early as possible, to identify process trends and the need for possible corrective action(s), and to ensure compliance to specifications. Quality audits all processing for the same purposes, but also to ensure proper recording, disposition of non-conforming materials and for the approval and implementation of proper corrective measures.

Vendor and Subcontractor Audit
Suppliers of direct materials to CCD Imaging are not audited provided their materials are accepted and conform to certificates of compliance, certificates of analysis, incoming inspection, specified use tests, or verification of composition and or construction. However, quality does initially approve and routinely audits all subcontractors that provide manufacturing, environmental and calibration services for CCD Imaging.

one of the following: return to vendor, use as is, scrap, rework/repair, or return to customer. Documentation accompanying non-conforming materials defines the discrepancy(s), cause (if known) and required corrective action to prevent or minimize recurrence. Quality assurance is responsible for coordinating the analysis and disposition of received material and material returned from customers that are non-conforming to specifications. CCD Imaging engineering and quality assurance are responsible for coordinating the analysis and disposition of non-conforming material detected during manufacturing or test and for implementing corrective action. Where contractually required, customer involvement and approval are obtained by quality assurance.